

# **JEDEC STANDARD**

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## **Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)**

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### **JESD22-A114D**

(Revision of JESD22-A114C.01, March 2005)

MARCH 2006

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**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



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**TEST METHOD A114D**  
**ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING**  
**HUMAN BODY MODEL (HBM)**

(From JEDEC Board Ballot JCB-00-27, JCB-04-103, JCB-04-104, JCB-04-105, JCB-05-137, and JCB-05-138 formulated under the cognizance of JC-14.1 Committee on Reliability Test Methods for Packaged Devices.)

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**1 Scope**

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This method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined electrostatic Human Body Model (HBM) discharge (ESD). The objective is to provide reliable, repeatable HBM ESD test results so that accurate classifications can be performed.

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**2 Apparatus**

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This test method requires the following equipment.

**2.1** An ESD pulse simulator and a Device Under Test (DUT) socket equivalent to the circuit of Figure 1. The simulator must be capable of supplying pulses with the characteristics required by Figure 2 and Figure 3.

**2.2 Oscilloscope**

The oscilloscope and amplifier combination shall have a 350 MHz minimum single-shot bandwidth and a visual writing speed of 4 cm/ns minimum.

**2.3 Current probe**

The current probe shall have a minimum pulse-current bandwidth of 350 MHz. The probe (transformer and cable with a nominal length of 1 meter) shall have a 1 GHz bandwidth, a minimum current rating of 12 amperes peak pulse-current capability and a rise time of less than one nanosecond.

**2.4 Evaluation loads**

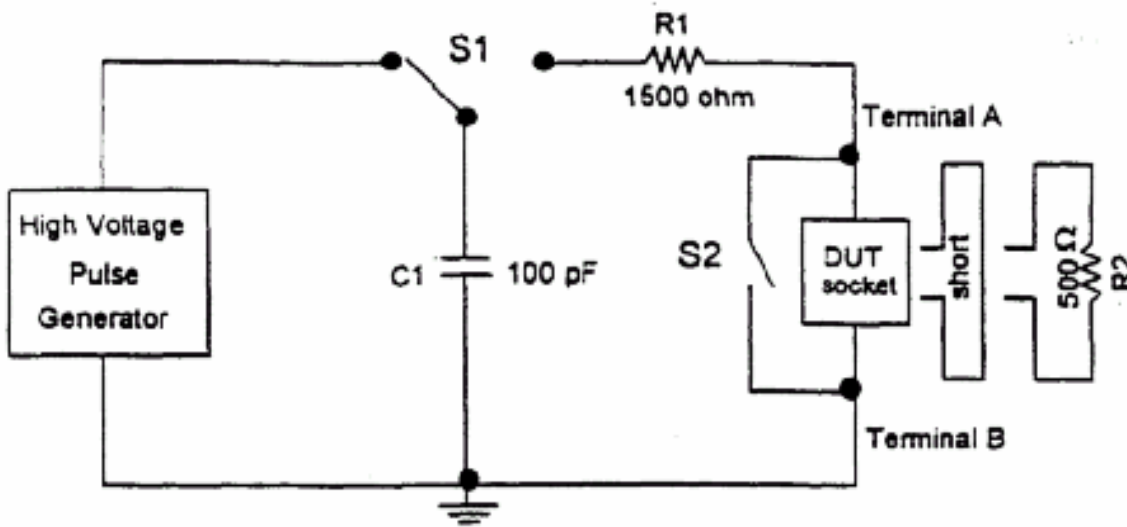
An 18-24 AWG tinned copper wire is recommended for the short waveform verification test. The lead length should be as short as practicable to span the distance between the two farthest pins in the socket while passing through the current probe. The ends of the wire may be ground to a point where clearance is needed to make contact on fine-pitch socket pins.

A 500  $\Omega$  +/-1%, 4000 V, low-inductance resistor shall be used for initial system checkout and periodic system recalibration.

## 2 Apparatus (cont'd)

### 2.5 Calibration

All apparatus used for tester evaluation shall be calibrated according to a documented, traceable calibration system and in accordance with manufacturer's recommendations.



**Figure 1 — Typical equivalent HBM ESD circuit**

NOTE 1 The performance of any simulator is influenced by its parasitic capacitance and inductance.

NOTE 2 Precautions must be taken in tester design to avoid recharge transients and multiple pulses.

NOTE 3 R2, used for initial equipment qualification and requalification as specified in 3.1, shall be a low inductance, 4000 V, 500  $\Omega$  resistor with +/-1% tolerance.

NOTE 4 Stacking of DUT socket adaptors (piggybacking) is allowed only if the waveforms can be verified to meet the specifications in Table 1.

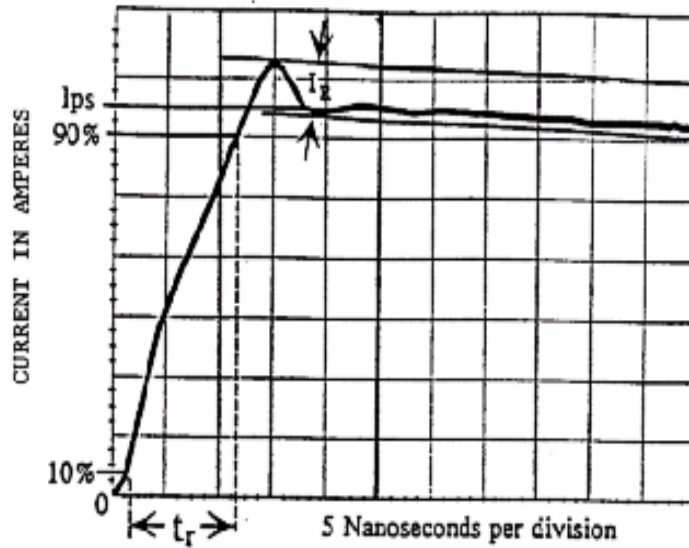
NOTE 5 Reversal of terminals A and B to achieve dual polarity is not permitted.

NOTE 6 S2 shall be closed at least 10 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state.

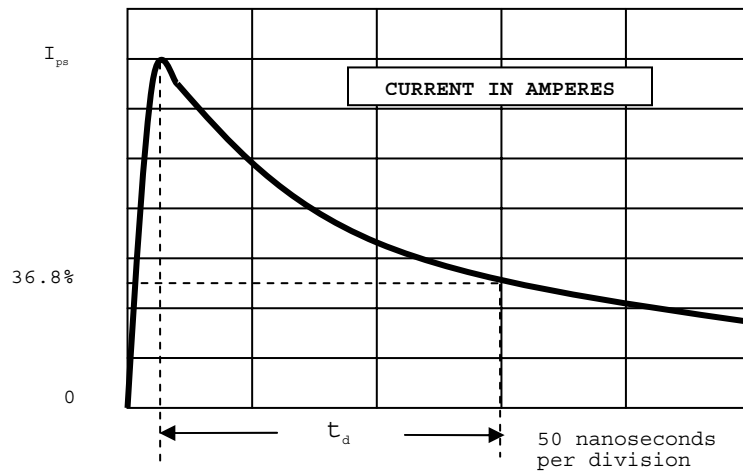
NOTE 7 R1, 1500  $\Omega$  +/- 1%.

NOTE 8 C1, 100 pF +/- 10% (effective capacitance).

2 Apparatus (cont'd)



(a) Pulse rise time, ( $t_r$ )



(b) Pulse decay time, ( $t_d$ )

Figure 2 — Current waveforms through a shorting wire

## 2 Apparatus (cont'd)

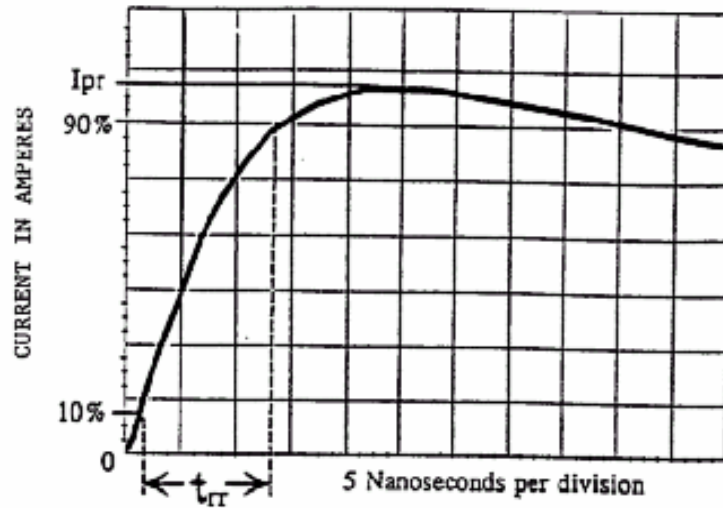


Figure 3 — Current waveform through a 500  $\Omega$  resistor\*

\* The 500  $\Omega$  load is used only during Equipment Qualification as specified in 3.1.

### 2.6 Optional trailing pulse detection apparatus

The following are required to conduct the optional trailing pulse detection in Figure 4.

1. A voltage probe with a minimum input impedance of 10M  $\Omega$ , a maximum capacitance of 10 pF, a minimum bandwidth of 1 MHz, and a minimum peak-to-peak voltage rating of 15 V.
2. A 10k  $\Omega$  +/- 1%, 4000 V resistor.
3. A Zener diode with breakdown voltage between 6 V and 15 V and a rating between ¼ watt and 1 watt.

## 2 Apparatus (cont'd)

Measurement setup:

- load = 10k ohm
- parallel Zener diode ( $V_{bd} \sim 10V$ )  
for probe/scope protection

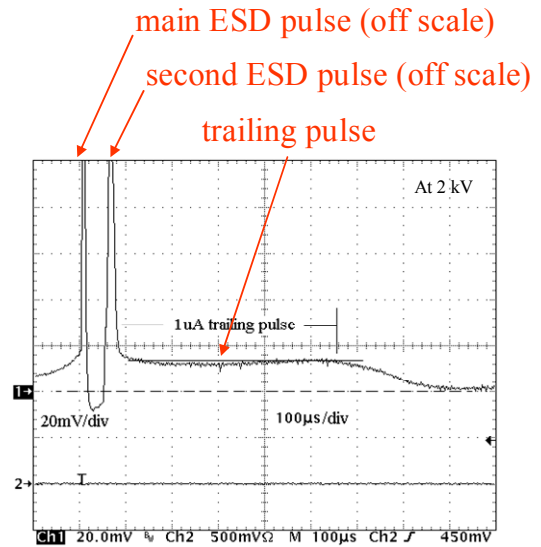
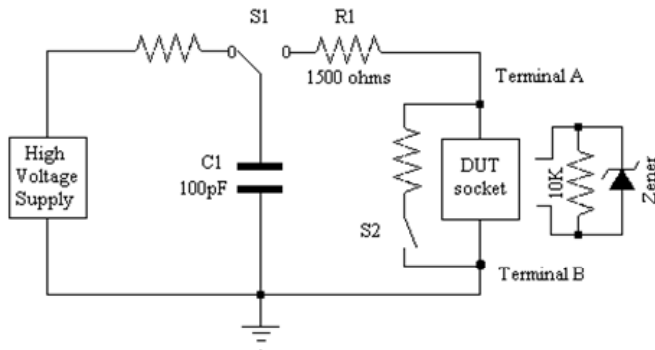


Figure 4 — Measurement setup and typical voltage waveform for detecting trailing EOS pulse (optional)

## 3 Qualification, calibration, and waveform verification

### 3.1 Equipment qualification

Equipment calibration must be performed during initial acceptance testing. Recalibration is required whenever equipment repairs are made that may affect the waveform and a minimum of every 12 months. The tester must meet the requirements of Table 1 and Figure 2 at all voltage levels, except 8000 V, using the shorting wire and at the 1000 V and 4000 V levels with the 500  $\Omega$  resistor (see Figure 3). The 8000 V level is optional. The waveform measurements during calibration shall be made using the worst-case pin on the highest pin count board with a positive mechanical clamp socket. (Machine repeatability should be verified during initial equipment acceptance by performing a minimum of 5 consecutive positive and a minimum of 5 consecutive negative waveforms at a voltage level in Table 2.)

The high-voltage relays and associated high-voltage circuitry shall be tested by the user of computer-controlled systems per the equipment manufacturer's instructions (system diagnostics). This test will check for any open or short relays.

### 3 Qualification, calibration , and waveform verification (cont'd)

**Table 1 — Waveform Specification**

Voltage Level (V)	I <sub>peak</sub> for Short†, I <sub>ps</sub> (A)	I <sub>peak</sub> for 500 Ω*, I <sub>pr</sub> (A)	Rise Time for Short, t <sub>r</sub> (ns)	Rise Time for 500 Ω*, t <sub>rr</sub> (ns)	Decay Time for Short, t <sub>d</sub> (ns)	Ringing Current I <sub>R</sub> (A)
250	0.15-0.19	N/A	2.0-10	N/A	130-170	15% of I <sub>ps</sub>
500	0.30-0.37	N/A	2.0-10	N/A	130-170	15% of I <sub>ps</sub>
1000	0.60-0.74	0.37-0.55	2.0-10	5.0-25	130-170	15% of I <sub>ps</sub>
2000	1.20-1.48	N/A	2.0-10	N/A	130-170	15% of I <sub>ps</sub>
4000	2.40-2.96	1.5-2.2	2.0-10	5.0-25	130-170	15% of I <sub>ps</sub> and I <sub>pr</sub>
8000 (optional)	4.80-5.86	N/A	2.0-10	N/A	130-170	15% of I <sub>ps</sub>

† I<sub>peak</sub> is the current through R1, that is, approximately V/1500 Ω.  
 \* The 500 Ω load is used only during equipment qualification as specified in 3.1.

#### 3.1.1 Safety training



During initial equipment set-up, the safety engineer or applicable safety representative, shall inspect the equipment in its operating location to ensure that the equipment is not operated in a combustible (hazardous) environment.

Additionally, all personnel shall receive system operational training and electrical safety training prior to using the equipment.

### 3 Qualification, calibration, and waveform verification (cont'd)

#### 3.1.2 Detection of trailing EOS pulse (optional)

Some HBM testers are known to produce a trailing electrical pulse. Some advanced technologies may be vulnerable to these pulses resulting in an electrical overstress (EOS). If trailing pulses are of concern for the technology under test, then any trailing pulse after the HBM pulse must be less than 4  $\mu\text{A}$  at positive and negative 4000 V level using the 10 k $\Omega$  load in parallel with the Zener diode, as shown in Figure 4. Scanning for the presence of any trailing pulse shall cover a period of at least 1 msec after the HBM pulse.

NOTE 1 The HBM pulse may show a slow decay of up to 100  $\mu\text{sec}$  to reach the 4  $\mu\text{A}$  specification level due to the use of a large load and the added capacitive parasitics in the measurement setup. This part of the slow decay shall be excluded in determining the trailing pulse magnitude.

NOTE 2 To determine if a device to be tested is susceptible to damage from the trailing pulse it may be necessary to measure the voltage across the actual device during HBM testing, or a circuit similar to that in Figure 4. If the circuit in Figure 4 is used the resistor should be changed from the 10 k $\Omega$  value to a value that simulates the device's properties and the Zener diode should be chosen to match the device's breakdown voltage. The measured voltage and the time that it is present on the device can then be compared to the known reliability mechanisms of the technology, such as time dependent dielectric breakdown (TDDB), to determine if a reliability concern is posed by the HBM tester. For sufficiently advanced technologies it may be necessary to use a criterion more stringent than the 4  $\mu\text{A}$  at 4000 V with a 10 k $\Omega$  resistor.

#### 3.2 Worst-case pin

The worst-case pin combination for each socket and DUT board shall be identified and documented. It is recommended that the manufacturers supply the worst-case pin data with each DUT board. The pin combination with the waveform closest to the limits (see Table 1) shall be designated for waveform verification.

3.2.1 The worst-case pin combination shall be identified by the following procedure.

3.2.1.1 For each test socket, identify the socket pin with the shortest wiring path from the pulse generating circuit to the test socket. Connect this pin to Terminal B (where it will remain the referenced pin throughout the worst-case pin search) and connect one of the remaining pins to Terminal A. Attach a shorting wire between these pins with the current probe around the shorting wire, as close to Terminal B as practicable.

3.2.1.2 Apply at least one positive 4000 V pulse and at least one negative 4000 V pulse and verify that the waveform meets the requirements defined in Table 1 for both positive and negative pulses.

3.2.1.3 Repeat steps 3.2.1.1 and 3.2.1.2 until all socket pins have been evaluated.

3.2.1.4 Determine the worst-case pin pair (within the limits and closest to the minimum or maximum parameter values as specified in Table 1) to be used for future waveform verification.

### 3.2 Worst-case pin (cont'd)

**3.2.1.5** For initial board check-out connect a 500  $\Omega$  resistor between the worst-case pins previously identified with the shorting wire in step 3.2.1.4. Apply a positive and negative 4000 V pulse and verify that the waveform meets the requirements defined in Table 1.

**NOTE** As an alternative to the worst-case pin search, the reference pin pair may be identified for each test socket of each test fixture. The reference pin combination shall be identified by determining the socket pin with the shortest wiring path from the pulse generating circuit to the test socket. Connect this pin to Terminal B and then connect the socket pin with the longest wiring path from the pulse generating circuit to the test socket to Terminal A (normally provided by the manufacturer). Attach a shorting wire between these pins with the current probe around the shorting wire. Follow the procedure in step 3.2.1.2. For the initial board check-out connect a 500  $\Omega$  resistor between the reference pins. Apply a positive and negative 4000 V pulse and verify the waveform meets the requirements defined in Table 1.

### 3.3 Waveform verification

The waveform verification should be performed at the beginning of each shift that a tester is operated and when a socket/DUT board is changed. If at any time the waveforms do not meet the requirements defined within Figure 2 and Table 1 at the 1000 V or 4000 V level, the testing shall be halted until the waveform is in compliance. Additionally, the system diagnostics test as defined in 3.1 for automated systems shall be performed prior to the beginning of each shift testing is done. The period between waveform checks may be extended providing test data supports the increased interval. In case the waveform no longer meets the limits in Table 1, all ESD testing performed after the previous satisfactory waveform check will be considered invalid.

- a) With the required DUT socket installed and with no part in the socket, attach a shorting wire in the DUT socket such that the worst-case pins are connected between Terminal A and Terminal B as shown in Figure 1. Place the current probe around the shorting wire.
- b) Initiate at least one positive pulse at the 1000 V level per Table 1 and Figure 2. Verify that all parameters meet the limits specified in Table 1 and Figure 2.
- c) Initiate at least one negative pulse at the 1000 V level per Table 1. Verify that all parameters meet the limits specified in Table 1 and Figure 2.
- d) Initiate at least one positive pulse at the 4000 V level per Table 1 and Figure 2. Verify that all parameters meet the limits specified in Table 1 and Figure 2.
- e) Initiate at least one negative pulse at the 4000 V level per table 1. Verify that all parameters meet the limits specified in Table 1 and Figure 2.

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## 4 Classification procedure

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The devices used for classification testing must have completed all normal manufacturing operations. Testing must be performed using an actual device chip. It is not permissible to use a test chip representative of the actual chip or to assign threshold voltages based on data compiled from a design library or via software simulations.

NOTE Test chip in this case means ESD test structure.

### 4.1 Parametric and functional testing

Prior to ESD testing, parametric and functional testing using conditions required by the applicable part drawing or test specification shall be performed on all devices submitted for ESD testing. Guard band testing is also permitted. The test devices shall be within the limits stated in the part drawing for these parameters.

### 4.2 Devices for each voltage level

A sample of 3 devices for each voltage level shall be characterized for the device ESD failure threshold using the voltage steps shown in Table 1. Finer voltage steps may optionally be used to obtain a more accurate measure of the failure threshold. ESD testing should begin at the lowest step in Table 1 but may begin at any level. However, if another higher starting voltage level is used and the device fails, testing shall be restarted with a fresh device at the next lowest level. The ESD test shall be performed at room temperature.

### 4.3 Stress level

Each sample of 3 devices shall be stressed at one voltage level using 1 positive and 1 negative pulse with a minimum of 100 milliseconds between pulses per pin for all pin combinations specified in Table 2. Longer intervals are permitted and should be used if the devices are expected to be vulnerable to cumulative effects. It is permitted to use a separate sample of 3 devices for each pin combination set specified in Table 2. It is permitted to further partition each pin combination set in Table 2 and use a separate sample of 3 devices for each subset within the pin combination set. It is permitted to use the same sample (3) at the next higher voltage stress level if all parts pass the failure criteria specified in clause 5 after ESD exposure to a specified voltage level.

### 4.4 Pin combinations

The pin combinations to be used are given in Table 2. The actual number of pin combination sets depends on the number of power pin groups. Power pins and Power Pin Groups are defined in 4.5. Programming pins that do not draw current should be considered as I/O pins (example:  $V_{pp}$  pins on memory devices). Active discrete devices (FETs, transistors, etc.) shall be tested using all possible pin-pair combinations (one pin connected to Terminal A, another pin connected to Terminal B) regardless of pin name or function. All pins which are not connected to the die shall be verified as such and left open (floating) at all times. Pins labeled as “no connect” that are electrically connected to the die shall be tested as non-supply I/O pins.

## **4 Classification procedure (cont'd)**

### **4.5 Power pins**

A power pin is defined as any pin intended to provide power to any portion of the circuit. While most power pins are labeled such that they can be easily recognized as power pins (examples: VDD, VDD1, VDD2, VDD\_PLL, VCC, VCC1, VCC2, VCC\_ANALOG, VSS, VSS1, VSS2, VSS\_PLL, VSS\_ANALOG, etc.), others are not and require engineering judgment based on their functions in the normal circuit operation (examples: Vbias, Vref, etc.).

Power pins that are directly connected by metal (inside the package) form a power pin group.

#### **4.5.1 Power pins connected on die**

Power Pin Groups that are connected by metal at the die level may be tied together and treated as a single node for Terminal B connection but must be treated as individual pins for Terminal A as shown in Table 2.

#### **4.5.2 Power pins connected on package plane**

For Power Pin Groups that are tied together through a common package plane, it is permitted to select one or more (arbitrary) pins to represent the group for stressing (Terminal A). The other pins in the group do not need to be stressed. In the test sequences where this power pin group is held at ground (Terminal B), it is permitted to have all the pins in the group tied together and connected to Terminal B or to have only the previously selected pin(s) connected to Terminal B with all other pins in the group left floating.

#### **4.5.3 Other power pin types**

Any pin that is intended to be pumped above the positive supply or below the negative supply of its circuit block must be treated as a power pin (example: positive and negative terminal pins connected to a charge pump capacitor).

Any pin that is connected to an internal power bus (or a power pin) by metal must be treated as a power pin (example: a Vdd sensing pin). In that case, the pin may be tied together with the power pin(s) connected to the same bus and treated as one pin for Terminal B connection even though it is labeled a different name.

Any pin that is intended to supply power to another circuit on the same chip must be treated as a power pin. However, if a pin intended to supply power to a circuit on another chip but not to any circuit on the same chip, it may be treated as a signal pin.

## **4.6 I/O to I/O**

If a device has non-supply pins that are connected on the die and bonded out to multiple separate pins, then these pins shall be stressed individually according to combination set N+1 with the remainder of these connected pins left floating.

#### 4 Classification procedure (cont'd)

##### 4.6 I/O to I/O (cont'd)

Pin combination set N+1 in table 2 specifies to stress each non-supply pin individually with all other remaining non-supply pins tied together and connected to terminal B (except for those non-supply pins that are metal connected to the pin under stress on the die, which will be left open). As an alternative to this method, it is permitted to partition the pins to be connected to terminal B into two or more subsets, such that each of these pins is a member of at least one subset. The pin connected to terminal A is to be stressed to each of these subsets separately.

##### 4.7 Alternative sample group

If a different sample group is ESD tested at each stress level, it is permitted to perform the dc parametric and functional ATE testing after all sample groups have been ESD tested.

**Table 2 — Pin Combinations Sets for Integrated Circuits**

<b>Pin Combination Set</b>	<b>Connect Individually to Terminal A</b>	<b>Connect to Terminal B (Ground)</b>	<b>Floating Pins (unconnected)</b>
1	All pins one at a time, except the pin(s) connected to Terminal B	First power pin group	All pins except PUT* and first power pin group
2	All pins one at a time, except the pin(s) connected to Terminal B	Second power pin group	All pins except PUT and second power pin group
3	All pins one at a time, except the pin(s) connected to Terminal B	Nth power pin group	All pins except PUT and Nth power pin group
4	Each Non-supply pin, one at a time.	All other Non-supply pins collectively except PUT	All power pins (see 4.6)
* PUT = Pin under test.			

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**5 Failure criteria**

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A part will be defined as a failure if, after exposure to ESD pulses, it no longer meets the part drawing requirements using parametric and functional testing. If testing is required at multiple temperatures, testing shall be performed at the lowest temperature first.

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**6 Classification criteria**

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All samples used must meet the test requirements of section 4 up to a particular voltage level in order for the part to be classified as meeting a particular sensitivity classification.

CLASS 0: Any part that fails after exposure to an ESD pulse of 250 V or less.

CLASS 1A: Any part that passes after exposure to an ESD pulse of 250 V but fails after exposure to an ESD pulse of 500 V.

CLASS 1B: Any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 1000 V.

CLASS 1C: Any part that passes after exposure to an ESD pulse of 1000 V, but fails after exposure to an ESD pulse of 2000 V.

CLASS 2: Any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

CLASS 3A: Any part that passes after exposure to an ESD pulse of 4000 V, but fails after exposure to an ESD pulse of 8000 V.

CLASS 3B: Any part that passes after exposure to an ESD pulse of 8000 V.

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**Annex A (informative) Differences between JESD22-A114D and JESD22-A114C.01**


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This table briefly describes most of the changes made to entries that appear in this standard, JESD22-A114D, compared to its predecessor, JESD22-A114C.01 (March 2005). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

<b>Page</b>	<b>Description of change</b>
9	In 4.4 changed last sentence from “All pins configured as “no connect” shall be tested as non-supply I/O pins.”, to “All pins which are not connected to the die shall be verified as such and left open (floating) at all times. Pins labeled as “no connect” that are electrically connected to the die shall be tested as non-supply I/O pins.”
10	In 4.5, second paragraph, removed “may be tied together and treated as one pin for Terminal B connection. Otherwise each power pin must be treated as a separate power pin.”, replaced with “form a power pin group.”
10	In 4.5, last three paragraphs became 4.5.3.
10	Added 4.5.1 and 4.5.2
10	New 4.6 added, 4.6 became 4.7.
11	Table 2 in 3 <sup>rd</sup> and 4 <sup>th</sup> columns; changed “pin(s)” to “pin groups”.

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**A.1 Differences between JESD22-A114C.01, compared to its predecessor, JESD22-A114C (January 2005)**

<b>Page</b>	<b>Description of change</b>
3	Figure 3b was deleted. It was approved for removal in the publication of JESD22-A114C, this was missed at the time of publication.

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**A.2 Differences between JESD22-A114C, compared to its predecessor, JESD22-A114-B (June 2000).**

<b>Page</b>	<b>Description of change</b>
3	Figure 2b was modified to show pulse decay time definition more clearly
3	Figure 3b was deleted since it is not used.
4	Inserted 2.6 to describe the equipment required for Trailing Pulse.
5	Figure 4 has been added to show the test set-up for Trailing EOS Pulse.
7	Inserted 3.1.2 to describe the test and give guidance on its applicability.
9	Added in 4 language stating clearly that ESD testing must be performed on samples of the actual chip being evaluated

**A.2 Differences between JESD22-A114C, compared to its predecessor, JESD22-A114-B (June 2000). (cont'd)**

<b>Page</b>	<b>Description of change</b>
9	In 4.3: Reduced minimum interval between zaps to 100 milliseconds. Longer intervals are still permitted.
9	In 4.3: Clarified that pin combination sets may be partitioned as far as necessary and performed on different devices to eliminate possible cumulative effects.
9	In 4.4: the following text was removed: "Like named power pins (VCC1, VCC2, VSS1, VSS2, GND, etc.) that are directly connected by metal (inside the package) may be tied together and treated as one pin for Terminal B connection. Otherwise, each power pin must be treated as a separate power pin." and replaced with "Power pins are defined in 4.5."
9	In 4.4: the following text was removed: "All pins configured as "no connect" pins shall be verified as "no connect" and left open (floating) at all times. Pins labeled "no connect", that in fact are connected, shall be tested as non-supply pins." and replaced with "All pins configured as "no connect" shall be tested as non-supply I/O pins."
10	Added 4.5: Clarified power pin definitions. Included pins connected to charge pump capacitors as power pins.



Standard Improvement Form

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1. I recommend changes to the following:

Requirement, clause number \_\_\_\_\_

Test method number \_\_\_\_\_ Clause number \_\_\_\_\_

The referenced clause number has proven to be:

Unclear  Too Rigid  In Error

Other \_\_\_\_\_

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2. Recommendations for correction:

\_\_\_\_\_  
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