



SP6025

Dual LLC Synchronous Rectifier

DESCRIPTION

The fundamental of SP6025 synchronous rectifier (SR) driver IC combines our U.S. patented methods that utilize the principle of “prediction” logic circuit and current mode. The IC deliberates previous cycle timing to linear control the SR in present cycle by “predictive” algorithm that makes adjustments to the turn-off time, in order to achieve maximum efficiency and avoid cross-conduction at the same time. Specially, SP6025 is designed for LLC applications, and variable switching frequency system.

The SP6025 is a dual, fast turn-off intelligent controller to drive two N-ch power MOSFETs in LLC resonant converters for synchronous rectification.

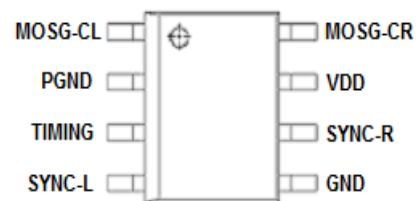
APPLICATIONS

- Storage area network power supplies
- Telecommunication converters
- Embedded systems
- Industrial & commercial systems using high current processors

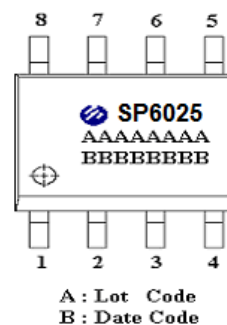
FEATURES

- Offers efficiency improvement over Schottky Diode.
- Low Standby Power to meet DOE Lot 6 Requirement.
- Dual gate driver for N-channel MOSFETs
- Prediction gate timing control.
- Minimum MOSFET body diode conduction.
- Self-detect DCM /CCM to enhance the performance under the variable switching frequency condition.
- Current mode operation in DCM, Prediction mode control in CCM.
- Operating frequency up to 250 KHz.
- Synchronize to transformer secondary voltage waveform.
- Rapid tacking function in prediction mode to adapt rapid load changing.
- Multi-blanking time to avoid the interference of turn on noise.

PIN CONFIGURATION (SOP-8)



PART MARKING

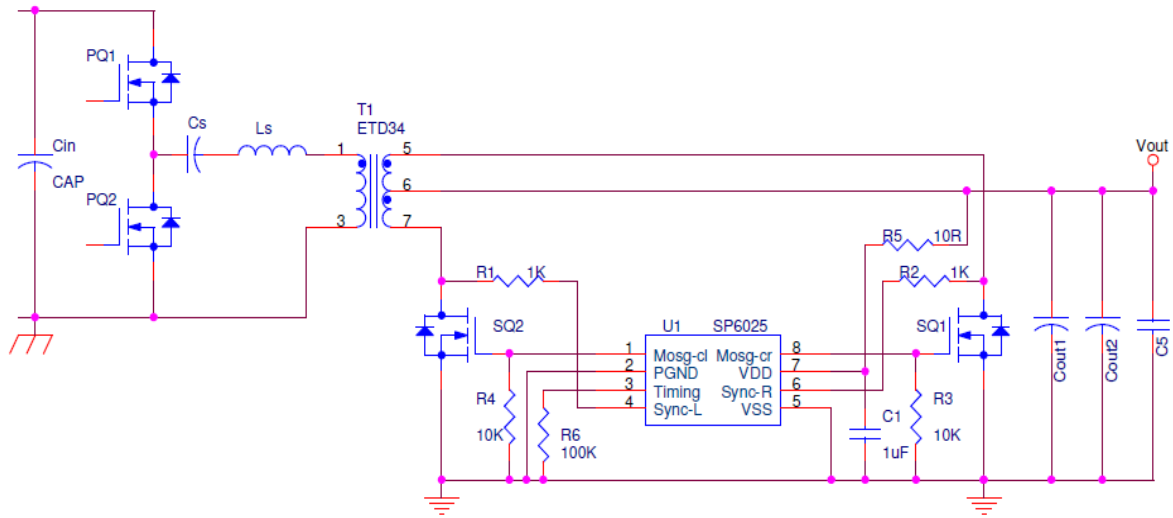




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TYPICAL APPLICATION CIRCUIT



PIN DESCRIPTION

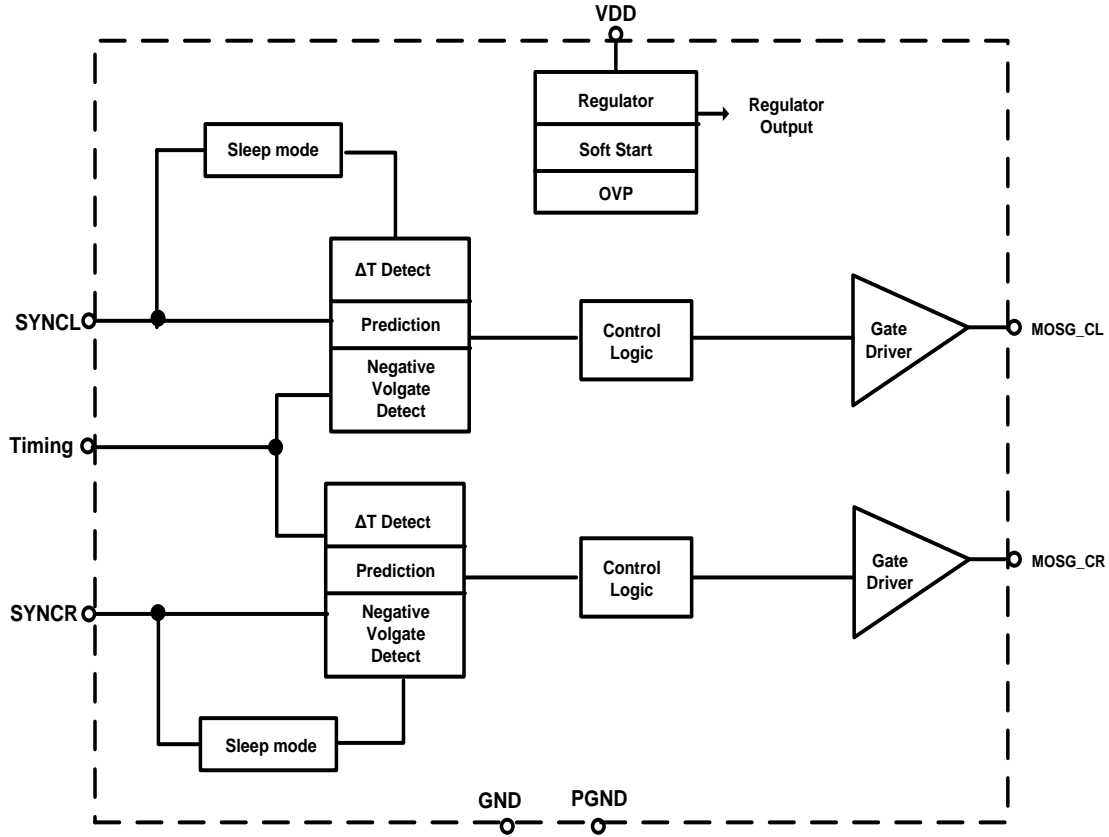
Pin	Symbol	Description
1	MOSG_CL	MOSFET_L gate driver.
2	PGND	Power ground connection.
3	TIMING	Discontinuous current filter timing adjustment resistor.
4	SYNC_L	Synchronized signal from the V_{DS} of SR MOSFET.
5	GND	Source pin ground connection.
6	SYNC_R	Synchronized signal from the V_{DS} of SR MOSFET.
7	VDD	DC supply voltage.
8	MOSG_CR	MOSFET_R gate driver.



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BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Part Marking
SP6025S8RGB	SOP-8	SP6025

※ SP6015S10RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified.)

The following ratings designate persistent limits beyond which damage to the device may occur.

Symbol	Paramete	Value	Unit
V _{DD}	DC Supply Voltage	40	V
SYNC-R/L	Sync input pin	40	V
MOSG-R/L	Output pin	12	V
TIMING	In/Out pin	5.5	V
I _{OUT}	Peak Source Current (Pulsed)	0.35	A
	Peak Sink Current (Pulsed)	2.0	A
P _D	Power Dissipation @ T _A =85°C (*)	0.45	W
T _J	Operating Junction Temperature Range	-40 to 125	°C
T _{STG}	Storage Temperature Range	-40 to 150	°C
T _{LEAD}	Lead Soldering Temperature for 5 sec.	260	°C

THERMAL RESISTANCE

Symbol	Paramete	Value	Unit
R _{ΘJA}	Thermal Resistance Junction to Ambient (*)	150	°C/W

(*)The power dissipation and thermal resistance are evaluated under copper board mounted with free air conditions.



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ELECTRICAL CHARACTERISTICS

($T_A=25^{\circ}\text{C}$, $V_{DD}=24\text{V}$, Freq. =50 KHz, Duty Cycle=50%, unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SUPPLY INPUT						
I_{DDH}	Supply current	No load		3		mA
		$V_{sync}=0\text{V}$, (Sleep mode)		0.22		mA
V_{DDH} Clamp	Clamp voltage	$I_{DD}=1\text{mA}$		37		V
		$I_{DD}=5\text{mA}$		38.5		V
V_{DDH} on	Enable voltage			3.5		V
V_{DD} hysteresis	Enable voltage			0.3		V
V_{OVP}	Over voltage protection			35		V
V_{OVP} hysteresis				3		V
SYNC REFERENCE (SYNC)						
V_{sync_on}	Turn-on threshold			-250		mV
V_{gate_low}	Gate pull low threshold			-35		mV
V_{sync_off}	Turn-off threshold			20		mV
I_{sync}	Sync input current				30	mA
CONTROL CIRCUIT SECTION						
T_{Don}	Turn-on delay	$C_{LOAD}=4.7\text{nF}$, $V_{GS}=2\text{V}$		210		nS
T_{Doff}	Turn-off total delay	$V_{SYNC}=0\text{V}$, $C_{LOAD}=4.7\text{nF}$, $R_{GATE}=0\Omega$, $V_{GS}=2\text{V}$		60		nS
T_{Bon}	Turn-on total blanking time			1		uS
V_{Boff}	Turn-off blanking V_{DS} threshold			1.8		V
T_{timing}	Falling slope detection timer V_{sync} from 1.8V to -50mV	$R_{timing}=100\text{K}\Omega$		130		nS
V_{timing}	Reference Voltage	$R_{timing}=100\text{K}\Omega$		1.2		V
T_{LL1}	Light-load-enter pulse width	SR MOS V_{DS} pulse width $<T_{LL1}$		1		uS
T_{LL-DEL}	Light-load-enter delay	Continuous counting cycles		4		cycle
T_{LL2}	Light-load-enter pause width	SR MOS V_{DS} pulse width $>T_{LL2}$		20		uS
T_{pred}	Prediction time	Fixed setting		200		nS
MOSFET GATE DRIVER(MOSG-C)						
V_{out_CCM}	Output clamp voltage in CCM			9.5		V
V_{out_DCM}	Output clamp voltage in DCM			6.5		V
T_r	Rise time	Load=4.7nF (*)		250		nS
T_f	Fall time	Load=4.7nF(*)		15		nS
	Pull up impedance	Peak current		14		Ω
	Pull down impedance			0.8		Ω

Notes:

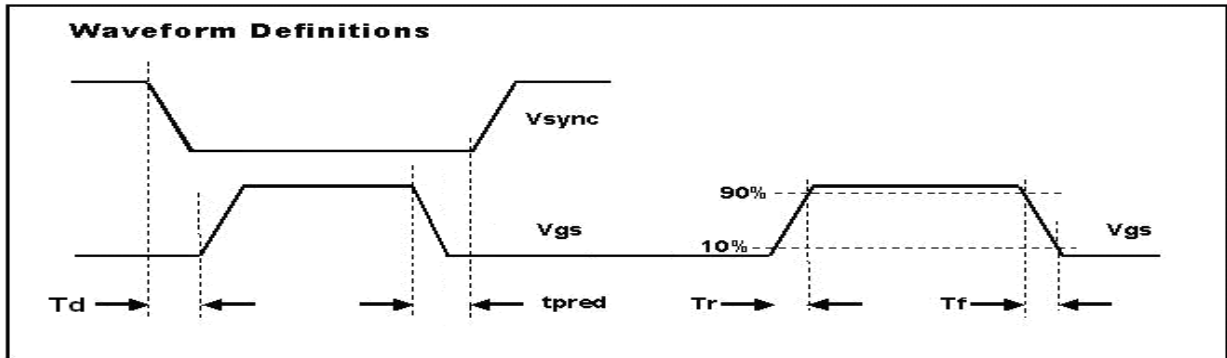
(*) Guaranteed by design and characterization



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PERFORMANCE CHARACTERISTICS ($T_A=25^{\circ}\text{C}$, unless otherwise specified.)





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