



SP6086H Synchronous Rectifier Driver

DESCRIPTION

The SP6086H is a low-drop diode emulator IC. By combining with an external switch, it replaces Schottky diodes in high-efficiency flyback converters.

The SP6086H generates its own supply voltage and does not need auxiliary winding for either high-side or low-side applications. Programmable ringing detection circuitry prevents the SP6086H from false turning on at V_{DS} oscillations during discontinuous conduction mode (DCM) and quasi-resonant (QR) operation. It has a timing pin to allow SP6086H to turn on at a selected load.

SP6086H is available in space saving SOT-23-6L package.

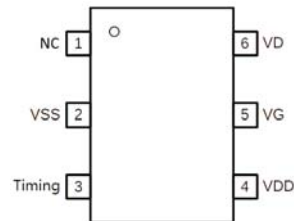
FEATURES

- Does not need auxiliary winding for either high-side or low-side applications
- Fast turn-on and turn-off delay
- Ringing detection prevents false turn-on during DCM and QR operations
- Less than 100mW standby power
- Up to 300KHz
- <400uA quiescent current at light load mode
- Supports CCM, DCM and QR operation
- Support both high-side and low-side rectification
- Available in space saving SOT-23-6L package

APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters
- USB PD Quick Chargers

PIN CONFIGURATION (SOT-23-6L)



PART MARKING

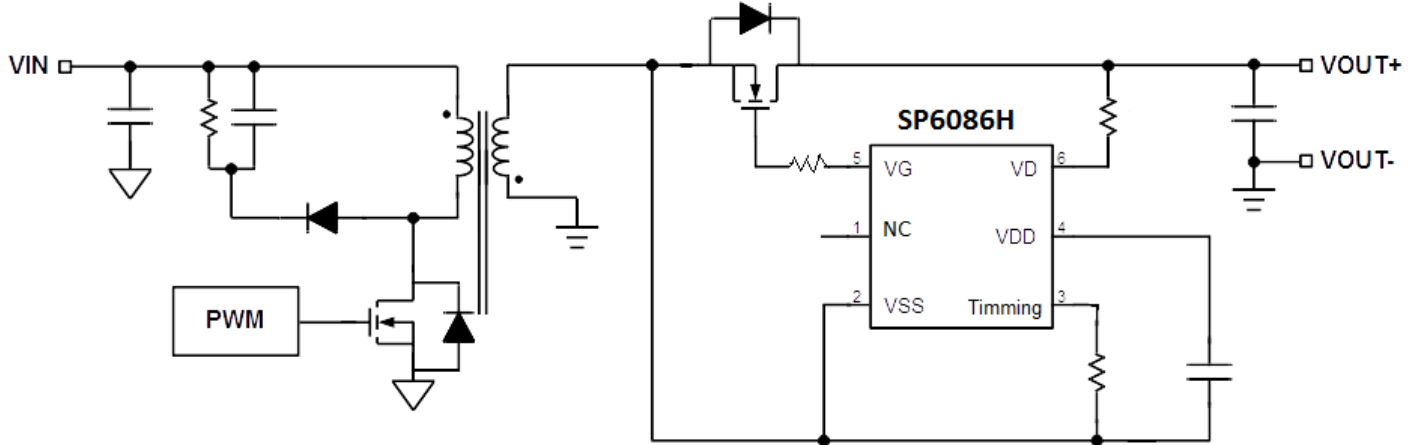




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TYPICAL APPLICATION CIRCUIT



PIN DESCRIPTION

Pin No.	Pin Name	Description
1	NC	
2	VSS	Ground, also used as reference for VD
3	Timing	Discontinuous current filter timing adjustment by a resistor
4	VDD	Linear regulator output. Supply voltage for internal circuits
5	VG	Gate driver output
6	VD	External FET drain voltage sensing and input of linear regulator

ORDERING INFORMATION

Part Number	Package	Part Marking
SP6086HS26RGB	SOT-23-6L	SP6086H

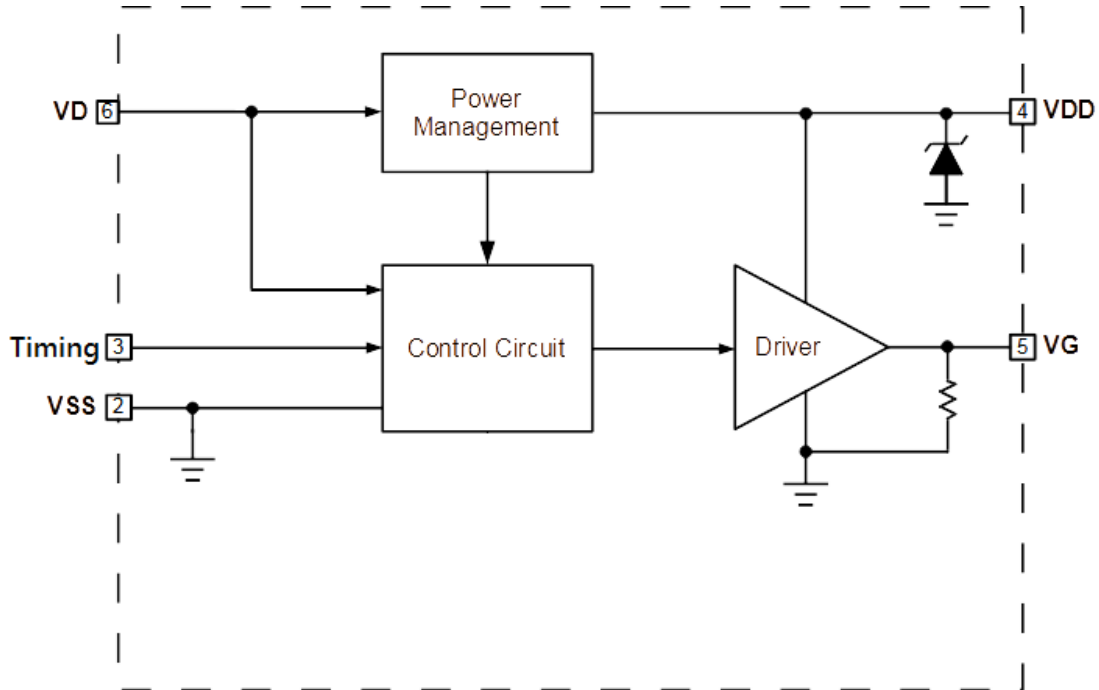
※ SP6086HS26RGB : Tape Reel ; Pb – Free ; Halogen – Free



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BLOCK DIAGRAM



The following ratings designate persistent limits beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V _{dd}	VDD, VG and SL pins voltages to VSS	-0.3 ~ 8.0	V
V _D	VD pin voltage to VSS	-0.7 ~ 200	V
P _D	Power Dissipation @ T _A =85°C (*)	0.3	W
T _J	Junction temperature	-40 ~ 150	°C
T _{STG}	Storage temperature	-40 ~ 150	°C
T _{LEAD}	Lead soldering temperature for 5 sec	260	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
R _{θJA}	Thermal Resistance Junction –to Ambient (*1)	220	°C/W
R _{θJC}	Thermal Resistance Junction –to Case (*2)	110	°C/W

(*1) θ_{JA} is measured in natural convection (still air) at T_A = 25°C with the component mounted on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

(*2) The power dissipation and thermal resistance are evaluated under copper board mounted with free air conditions



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ELECTRICAL CHARACTERISTICS

($T_A=25^{\circ}\text{C}$, $V_{DD}=5.5\text{V}$, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Section						
UVLO	VDD UVLO rising		4.5	4.9	5.3	V
	VDD UVLO Hysteresis			1.2		V
	VDD clamp voltage	$I_{DD} = 10\text{mA}$		7.5		V
I_{VD}	VDD charging current	$V_D = 20\text{V}$, $V_{DD} = 0\text{V}$		20		mA
		$V_D = 20\text{V}$, $R_{VDD}=1\text{K}\Omega$		7		mA
	VDD regulation voltage	$V_D = 20\text{V}$	6	6.3	6.5	V
I_{CC}	Operating current	$C_{LOAD}=4.7\text{nF}$, $F_{SW}=50\text{kHz}$		5		mA
	Shutdown current	$V_{DD}=\text{UVLO} - 0.5\text{V}$			140	uA
$I_{STANDBY}$	Light-load mode current	$R_{\text{timing}}=100\text{k}\Omega$		250	400	uA
Control Circuitry Section						
V_{LL-DS}	VSS-VD turn-on threshold			230		mV
V_{fwd}	VSS-VD forward voltage			25		mV
	VSS-VD turn-off threshold			3		mV
T_{Don}	Turn-on delay	$C_{LOAD}=5\text{nF}$, $V_{GS}=2\text{V}$			75	ns
		$C_{LOAD}=10\text{nF}$, $V_{GS}=2\text{V}$			100	ns
	Turn-off propagation delay(*)	$V_D=V_{SS}$		15		ns
T_{Doff}	Turn-off total delay	$V_D=V_{SS}$, $C_{LOAD}=5\text{nF}$, $R_{GATE}=0\Omega$, $V_{GS}=2\text{V}$		30		ns
		$V_D=V_{SS}$, $C_{LOAD}=10\text{nF}$, $R_{GATE}=0\Omega$, $V_{GS}=2\text{V}$		40		ns
T_{Bon}	Turn-on blanking time			0.7		us
V_{Boff}	Turn-off blanking V_{DS} threshold		1.5		2.5	V
T_{timing}	Falling slope detection timer	$R_{\text{timing}}=100\text{k}\Omega$, V_D transition from 2V to -0.1V		30		ns
V_{timing}	Reference voltage	$R_{\text{timing}}=100\text{k}\Omega$,	0.95	0.985	1.01	V
T_{LL1}	Light-load-enter pulse width			0.8		us
T_{LL1-H}	Light-load-enter pulse width hysteresis			0.3		us
T_{LL2}	Light-load-enter pause width			1		ms
T_{LL-DEL}	Light-load-enter delay			6		cycle
Gate Driver Section						
V_{G-L}	Gate output low voltage	$I_{LOAD}=1\text{mA}$			0.1	V
V_{G-H}	Gate output high voltage		6			V
	Peak source current(*)			0.5		A
	Peak sink current(*)			3		A
	Pull down impedance			1		Ω

Notes:

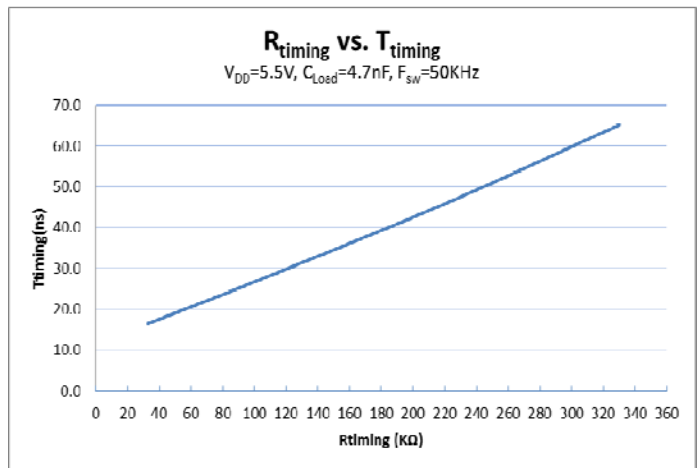
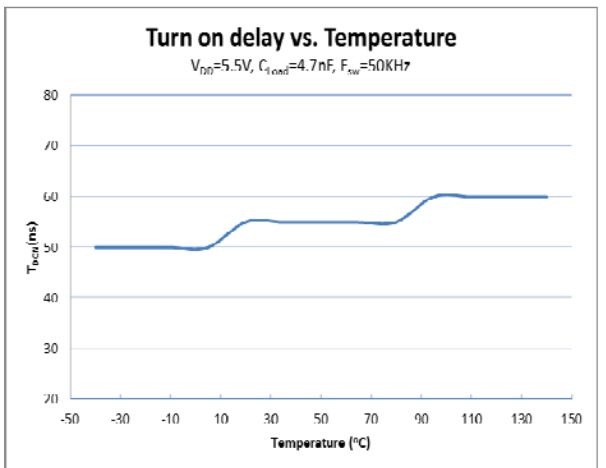
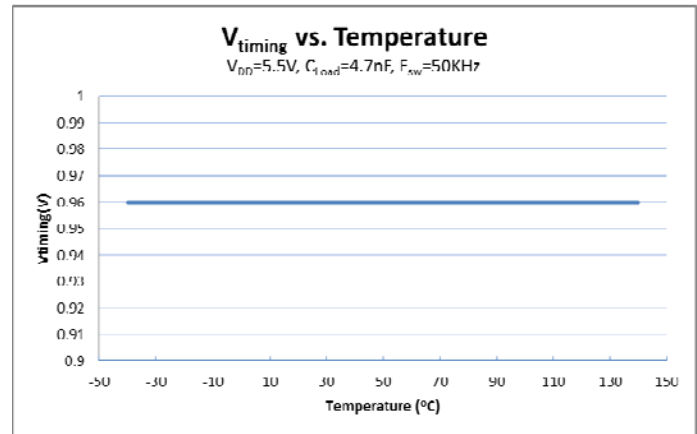
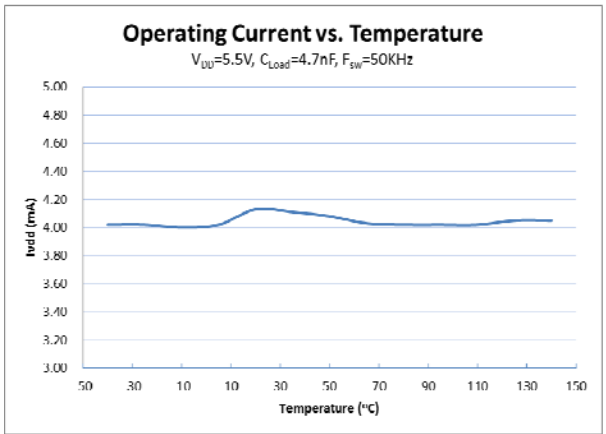
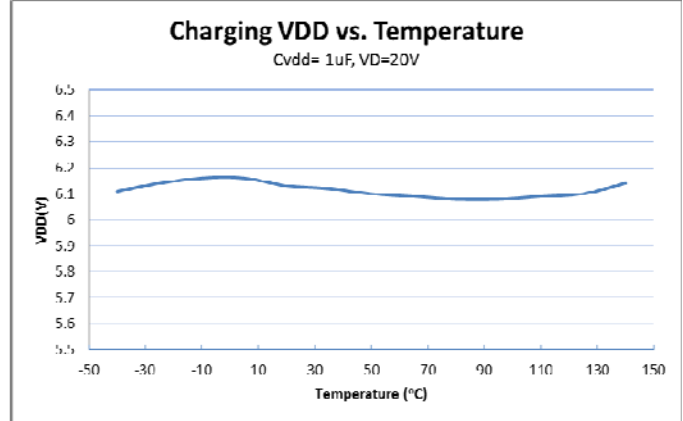
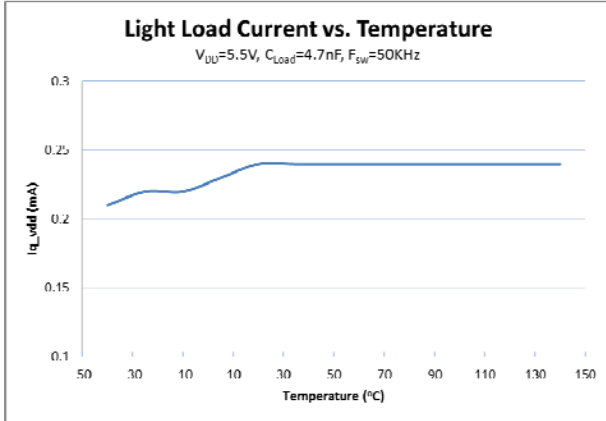
(*)Guaranteed by design and characterization.



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TYPICAL CHARACTERISTICS





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SYNC Power Corporation
7F-2, No.3-1, Park Street
NanKang District (NKSP), Taipei, Taiwan, 115,
R.O.C Phone: 886-2-2655-8178
Fax: 886-2-2655-8468