



SP6892

Quasi-Resonant with Silicon Rectifier Controller

DESCRIPTION

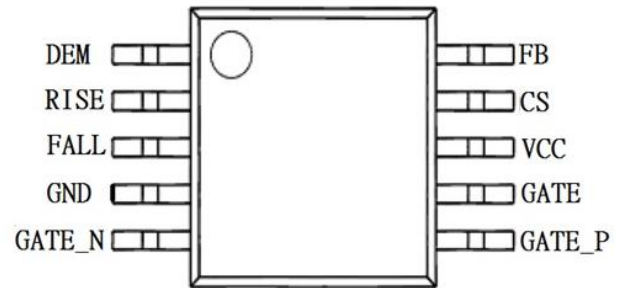
SP6892 is a highly integrated flyback multimode QR controller with the SR controller. With the patented technology, SP6892 is placed in the Primary side of the power supply provides fast and better control for the SR MOSFET turning ON and OFF. Through pulse transformer, SP6892 transfers the ON and OFF signal to the secondary side and eliminates the crossing between primary side MOSFET and the secondary side MOSFET.

SP6892 is offered in space saving SOP-10 pack design.

APPLICATIONS

- AC/DC switching power adaptor
- Set-top box power supply
- Open-frame switching power supply
- NB Adaptor
- TV/Monitor Standby Power
- PC Peripherals

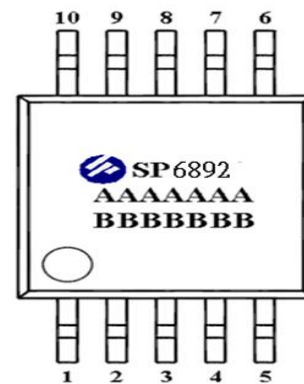
PIN CONFIGURATION (SOP-10)



FEATURES

- Internal soft start reducing MOS FET VDS stress
- Multi-mode operation for better efficiency
- Frequency shuffling for better EMI
- Extended burst mode for lower standby power loss
- The rich set of protection features:
 - VCC Under Voltage Lockout (UVLO) with hysteresis
 - VCC Over Voltage Protection (VCC OVP) and clamp
 - Cycle-by-cycle current limiting with line voltage compensation
 - Over Load Protection (OLP) with auto-recovery
 - Adjustable load Over Voltage Protection (OVP)
 - Fixed on-chip and adjustable external over temperature protection (OTP) with auto-recovery
- Build-in synchronous rectifier optimized for switching power system.
- SOP-10 package design

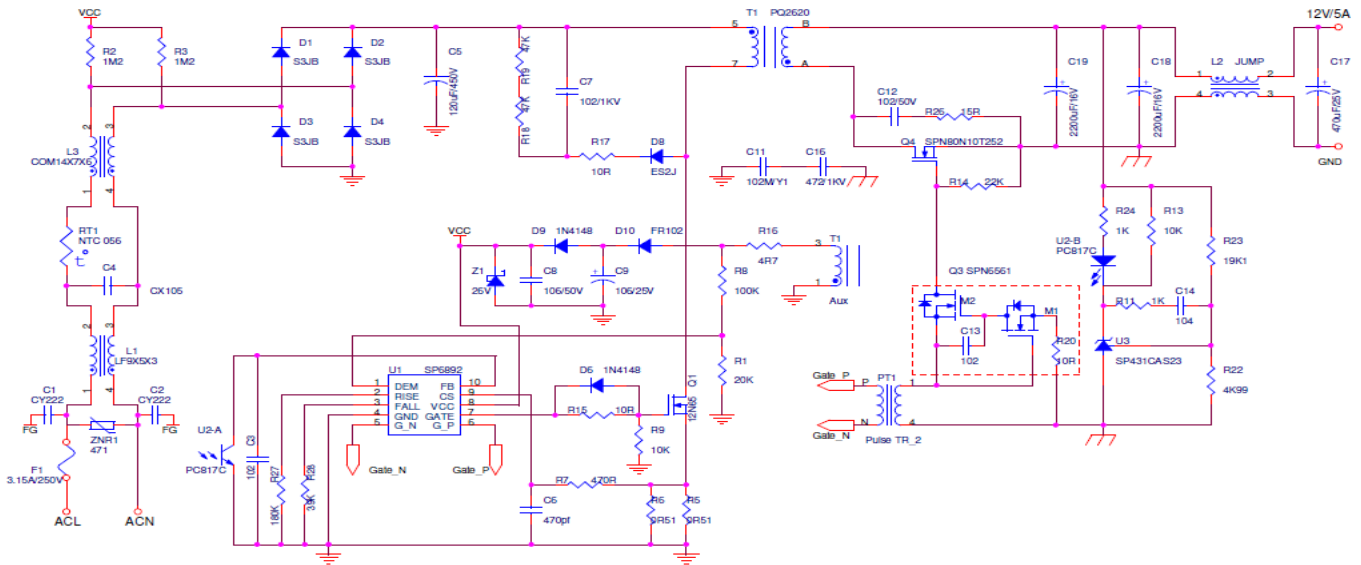
PART MARKING





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TYPICAL APPLICATION CIRCUIT



PIN DESCRIPTION

Pin No.	Pin Name	Description
1	DEM	Core reset detection and output OVP
2	RISE	GATE_P pulse width setting
3	FALL	GATE_N pulse width setting
4	GND	Ground
5	GATE_N	SR negative gate control signal
6	GATE_P	SR positive gate control signal
7	GATE	PWM gate driver output to drive the external MOSFET
8	VCC	Supply voltage for the IC
9	CS	Current sense and external OTP through a NTC resistor
10	FB	Voltage feedback

ORDERING INFORMATION

Part Number	Package	Part Marking
SP6892S10RGB	SOP-10	SP6892

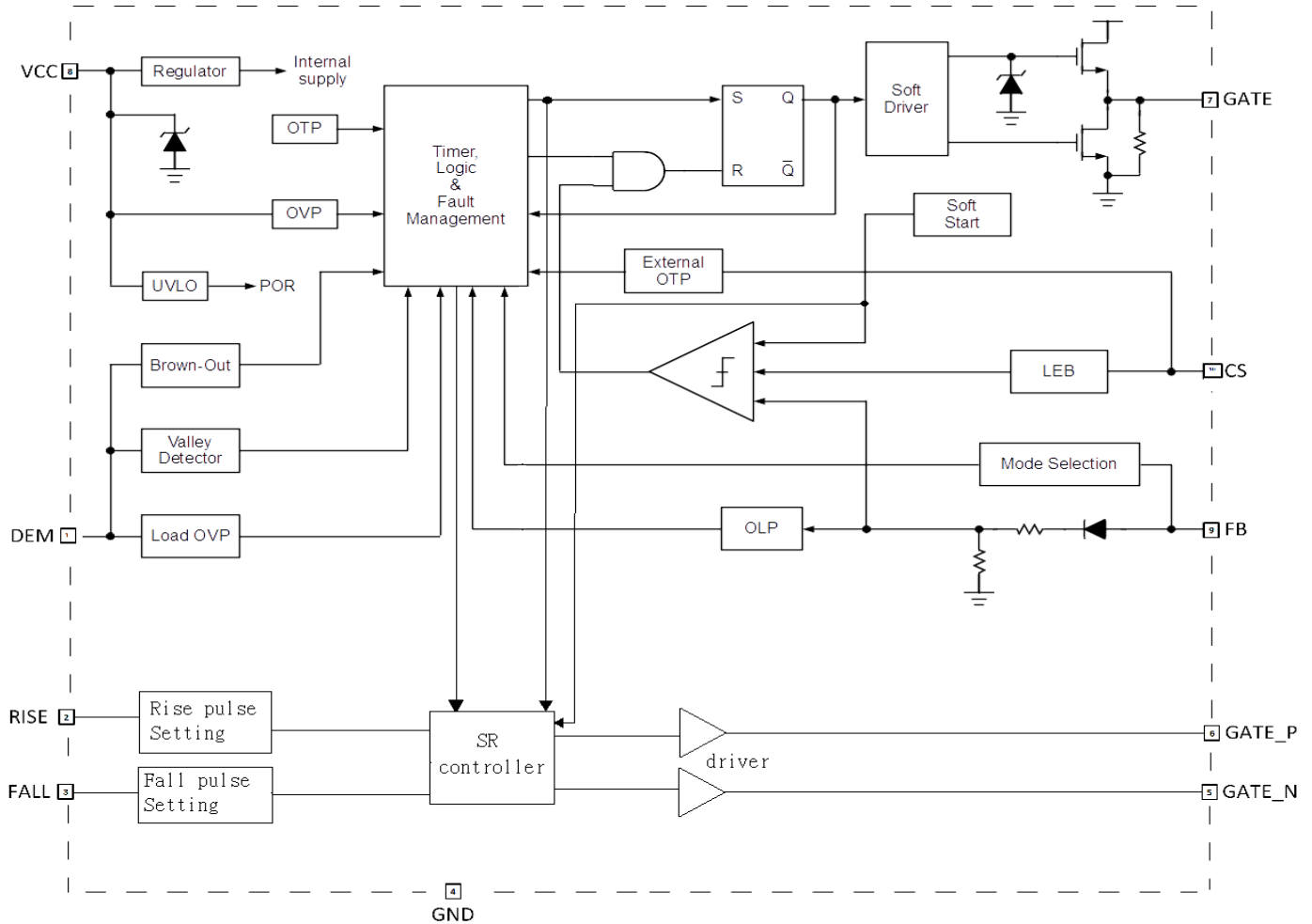
※ SP6892S10RGB : Tape Reel ; Pb – Free ; Halogen – Free



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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

The following ratings designate persistent limits beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V _{CC}	Zener clamp voltage (@ 10mA)	31	V
V _{FB} , V _{CS} , V _{DEM}	FB, CS, DEM pin voltage	-0.3 ~ 7.0	V
T _{OP}	Operating ambient temperature	-40 ~ 85	°C
T _J	Operating junction temperature	-40 ~ 150	°C
T _{STG}	Storage temperature	-40 ~ 150	°C
T _{LEAD}	Lead soldering temperature for 5 sec	260	°C
THERMAL RESISTANCE			
R _{ΘJC}	Thermal Resistance Junction – Case (*)	110	°C/W



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ELECTRICAL CHARACTERISTICS

($T_A=25^{\circ}\text{C}$, $V_{CC}=16\text{V}$, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage Section (VCC pin)						
I _{startup}	Start-up current	$V_{CC}=\text{UVLO}(\text{OFF})-1.5\text{V}$	0.5	2	7	uA
I _{cc(op)}	Operating current	$V_{FB}=3\text{V}$	1	2	3.5	mA
		$V_{FB}=3\text{V}$, $C_L=1\text{nF}$		3	5	mA
		$V_{FB}=3\text{V}$, $C_L=4.7\text{nF}$		7	10	mA
I _{cc(burst)}	Burst mode operating current	$V_{FB}=0.5\text{V}$, $V_{CS}=0\text{V}$	0.1	0.6	0.8	mA
UVLO(ON)	VCC under voltage lockout enter		7	8.5	10	V
UVLO(OFF)	VCC under voltage lockout exit (recovery)		17	18.5	21	V
OVP	VCC over voltage protection		26	28	30	V
Feedback Section (FB pin)						
I _{FB(SC)}	Short circuit current		100	250	400	uA
V _{FB_Open}	Open loop voltage		4.5	5.3	6.1	V
V _{TH_BM_off}	Burst mode exit threshold		0.65	0.8	0.95	V
V _{TH_BM_on}	Burst mode enter threshold		0.55	0.7	0.85	V
V _{FB(OLP)}	Over load protection threshold			4.4		V
T _{DEL(OLP)}	Over load protection delay			80		mS
Demagnetization Detection Section (DEM pin)						
V _{DEM(TH)}	Demagnetization threshold			75		mV
V _{DEM(H)}	Upper clamp voltage		5.8	6.2	6.5	V
V _{DEM(L)}	Lower clamp voltage		-1.5	-0.7		V
T _{DEL(DEM)}	Demagnetization propagation delay			250		nS
V _{DEM(OVP)}	Load over voltage protection threshold		3.2	3.75	4.3	V
T _{DEL(OVP)}	Number of subsequent cycles to trigger OVP			4		Cycle
I _{B(in)}	Brown-in current threshold		60	110	150	uA
I _{B(out)}	Brown-out current threshold		40	90	140	uA
T _{B(in)}	Number of cycles to detect brown-in			4		Cycle
T _{B(out)}	Brown-out De-bounce time			50		ms
Current Sense Section (CS pin)						
V _{CS(L)}	CS threshold at zero duty cycle	$V_{FB}=3\text{V}$	0.415	0.45	0.485	V
V _{CS(H)}	CS threshold at max duty cycle	$V_{FB}=3\text{V}$		0.8		V
V _{CS(BM)}	CS threshold at burst mode	$V_{FB}=1\text{V}$	0.2	0.3	0.4	V
T _{LEB}	Leading edge blanking time			300		nS
T _{DEL(CS)}	Over current detection and control delay			80		nS
V _{TH(OTP)}	External OTP threshold			0.25		V
T _{DEL(OTP)}	External OTP debounce time			50		mS
Soft Start Section						
T _{SS}	Soft start time			4		mS
Internal OTP						
T _{SD}	Thermal shutdown threshold			150		°C
T _{SD_HYS}	Thermal shutdown hysteresis			30		°C



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ELECTRICAL CHARACTERISTICS (continued)

(T_A=25°C, V_{CC}=16V, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator						
F _{BURST}	Burst mode switching frequency		10	22	25	kHz
F _{QR(L)}	Frequency low clamp in QR mode		47	52	57	kHz
F _{QR(H)}	Frequency high clamp in QR mode			75		kHz
G_PFM	Frequency reduction ratio			60		kHz/V
ΔF _{(shuffle)/F}	Frequency shuffling range		-4		+4	%
T _{ON}	Maximum ON time		10	12.5	15	uS
T _{OFF}	Maximum OFF time		40	55	75	uS
Gate Driver Section (GATE pin)						
V _{O(L)}	Output low voltage	I _O =10mA			1	V
V _{O(H)}	Output high voltage		11.5			V
V _{O(CLAMP)}	Output clamp voltage	V _{CC} =20V		16.5		V
t _r	Voltage rise time	C _L =1nF		100		nS
t _f	Voltage fall time	C _L =1nF		50		nS
SR Section						
V _{RISE}	Reference voltage of rising pin	V _{CC} =20V	1.4	1.45	1.6	V
V _{FALL}	Reference voltage of rising pin	V _{CC} =20V	1.4	1.45	1.6	V
T _{GATE_P}	SR positive gate control signal	R=33KΩ	50	130	150	nS
T _{GATE_N}	SR negative gate control signal	R=33KΩ		130		nS

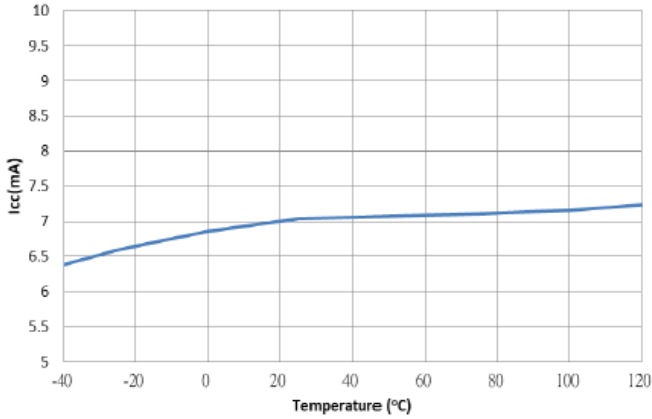


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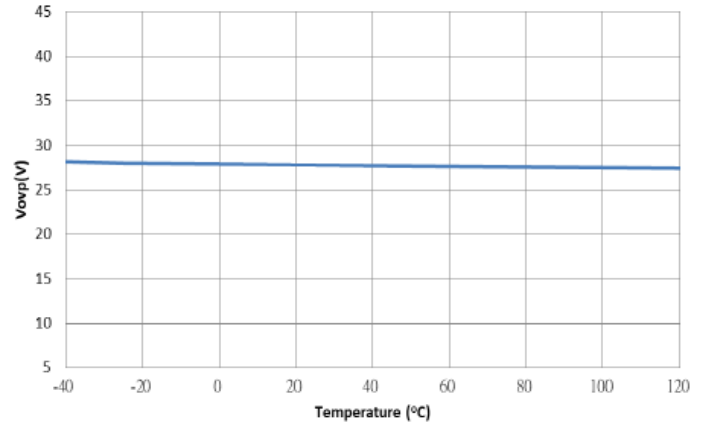
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PERFORMANCE CHARACTERISTICS (TA=25°C, unless otherwise specified.)

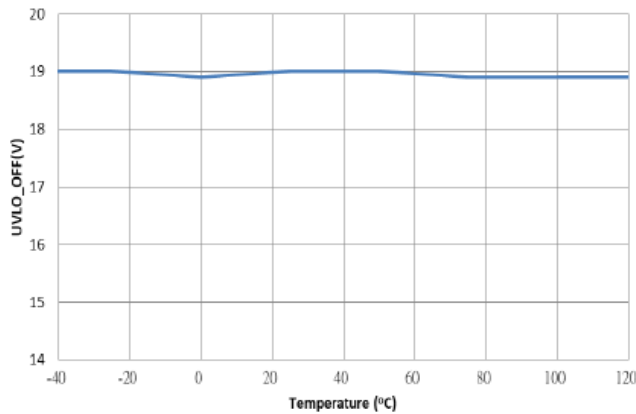
I_{CC} vs Temperature (load=4.7nF)



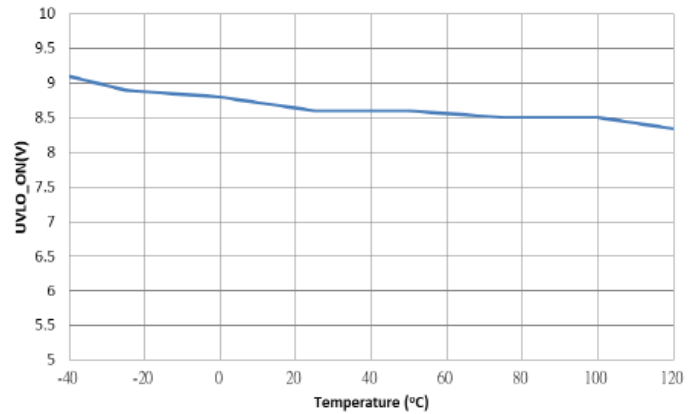
V_{ovp} vs Temperature



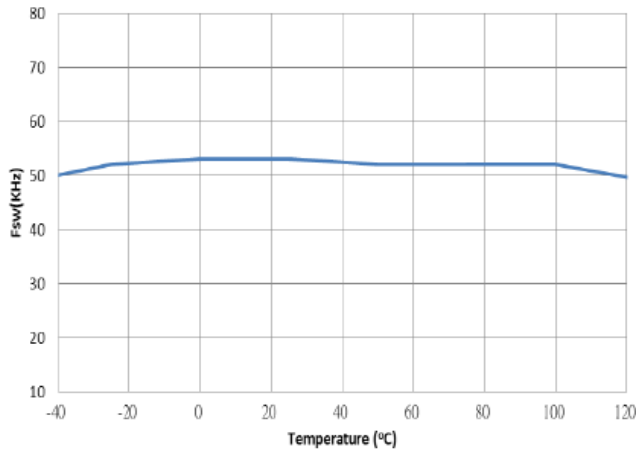
UVLO(OFF) vs Temperature



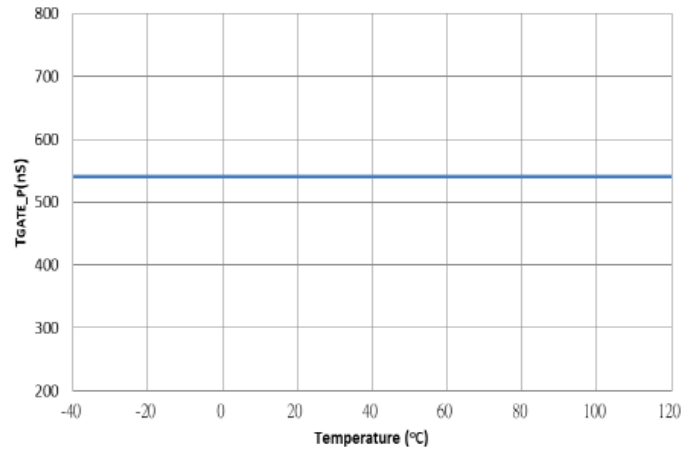
UVLO(ON) vs Temperature



F_{sw}(KHz) vs Temperature



T_{GATE_P}(nS) vs Temperature (R_{rise}=150KΩ)



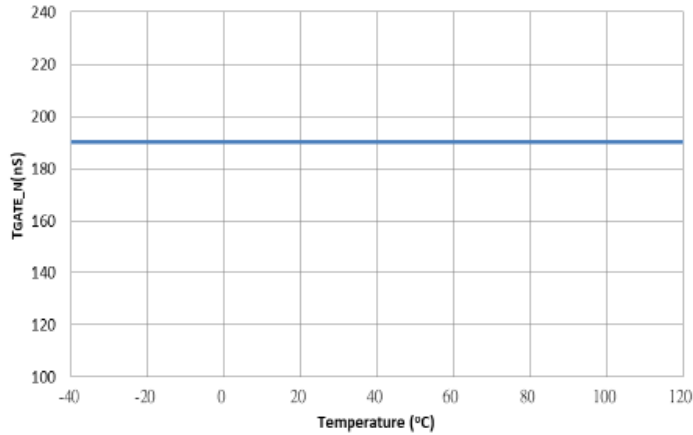


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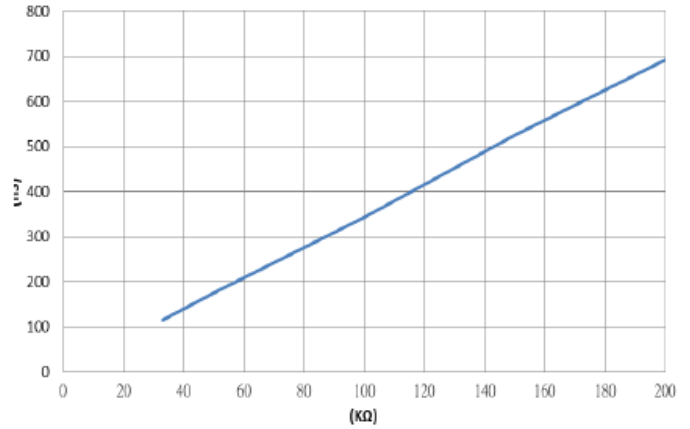
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PERFORMANCE CHARACTERISTICS (TA=25°C, unless otherwise specified.)

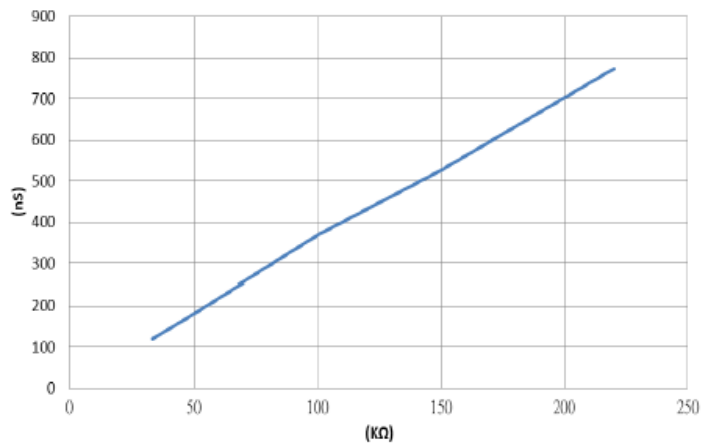
TGATE_N(nS) vs Temperature (R_{fall}=51KΩ)



R_{rise} vs. the pulse width of Gate_P



R_{fall} vs. the pulse width of Gate_N





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