SPE0332
2-Line ESD Protection Array

DESCRIPTION
The SPE0332 are designed by TVS bi-direction device that is to protect sensitive electronics from damage or latch-up due to ESD. They are designed for use in applications where board space is at a premium. SPE0332 will protect 2-line, and may be used on line where the signal polarities swing above and below ground.

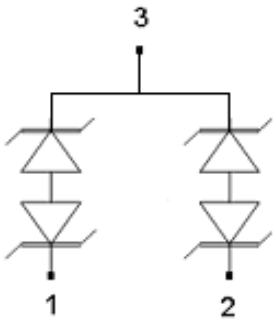
SPE0332 offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

SPE0332 may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small SOT-23 package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

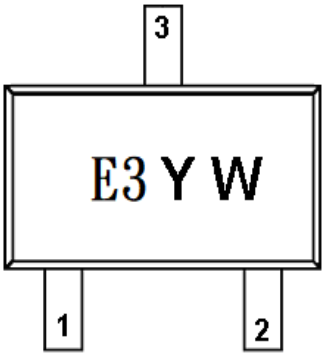
APPLICATIONS
- Cellular Handsets and Accessories
- Cordless Phone
- Communication systems
- Notebooks and Handhelds
- Portable Instrumentation
- Audio and video equipment
- Subscriber Identity Module (SIM) card protection

FEATURES
- ESD protection of two lines
- Max. peak pulse power: PPP = 350 W
- Low clamping voltage: VCL = 26 V
- Small SMD plastic package
- Ultra low leakage current: IRM < 90 nA
- ESD protection up to 23 kV
- IEC 61000-4-2, level 4 (ESD)
- IEC 61000-4-5 (surge); IPP = 15 A

PIN CONFIGURATION (SOT-23)



PART MARKING



Y : Year Code
W : Week Code

SPE0332
2-Line ESD Protection Array

ORDERING INFORMATION

Part Number	Package	Part Marking
SPE0332S23RGB	SOT-23	E3YW

※ SPE0332S23RGB : Tape Reel ; Pb – Free; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Peak Pulse Power (tp = 8/20 μs)	Ppk	350	W
Maximum Peak Pulse Current (tp = 8/20 μs)	Ipp	15	A
ESD per IEC 61000 – 4 – 2 (Air)	Vpp	±15	KV
ESD per IEC 61000 – 4 – 2 (Contact)	Vpp	±8	KV
Operating Junction Temperature	T_J	-65 ~ 150	℃
Storage Temperature Range	T_{STG}	-65 ~ 150	℃
Lead Soldering Temperature	T_L	260 (10sec)	℃

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Reverse Stand – Off Voltage	V_{RWM}				3.3	V
Reverse Breakdown Voltage	V_{BR}	It=5mA	5.8	6.4	6.9	V
Reverse Leakage Current	I_R	V_{RWM}=3.3V , T=25℃		0.09	2	μA
Differential Resistance	Rdif	I_R=1mA			400	Ω
Clamping Voltage	V_C	Ipp=1A , tp = 8/20 μs			8	V
Clamping Voltage	V_C	Ipp=15A , tp = 8/20 μs			26	V
Junction Capacitance	Cj	Between I/O Pin and GND V_R=0V , f=1MHz		101		pF

TYPICAL CHARACTERISTICS

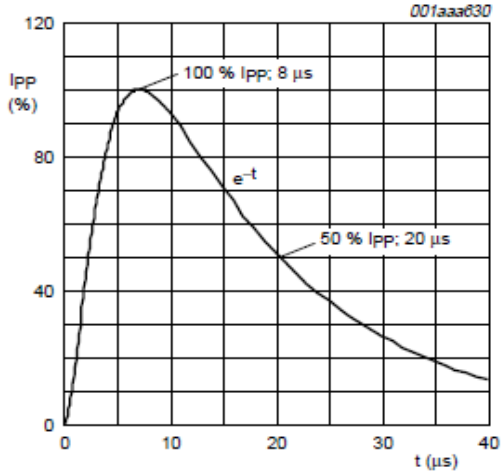


Fig 1. 8/20 µs pulse waveform according to IEC 61000-4-5

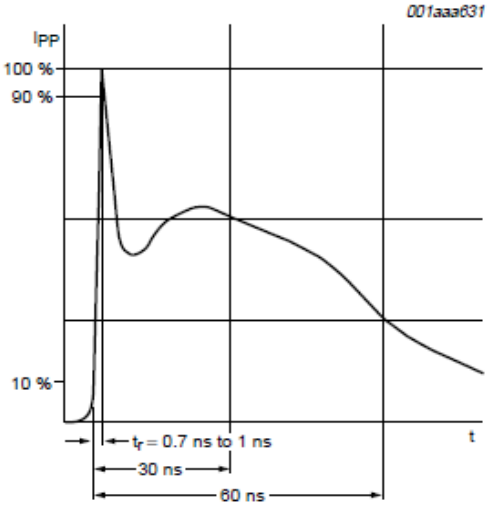
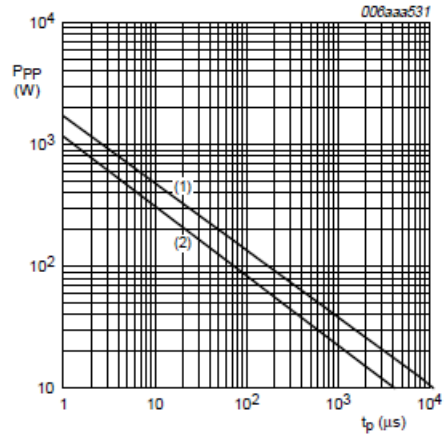


Fig 2. ESD pulse waveform according to IEC 61000-4-2

TYPICAL CHARACTERISTICS



T_{amb} = 25 °C

(1) PESD3V3L2BT and PESD5V0L2BT

(2) PESD12VL2BT, PESD15VL2BT, PESD24VL2BT

Fig 3. Peak pulse power as a function of exponential pulse duration t_p; typical values

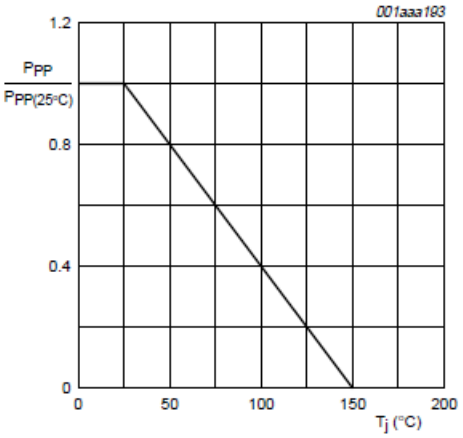
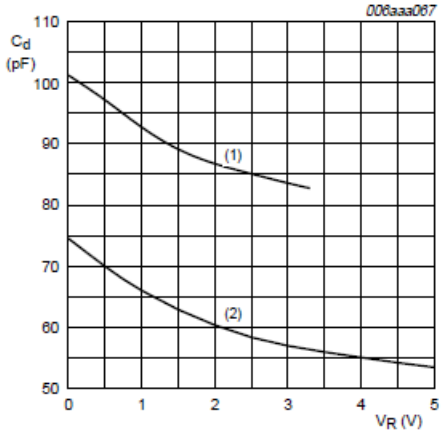


Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values

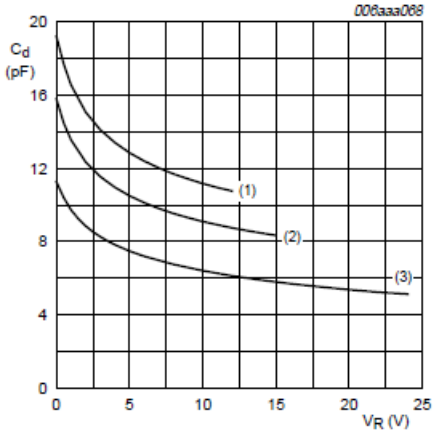


T_{amb} = 25 °C; f = 1 MHz

(1) PESD3V3L2BT

(2) PESD5V0L2BT

Fig 5. Diode capacitance as a function of reverse voltage; typical values



T_{amb} = 25 °C; f = 1 MHz

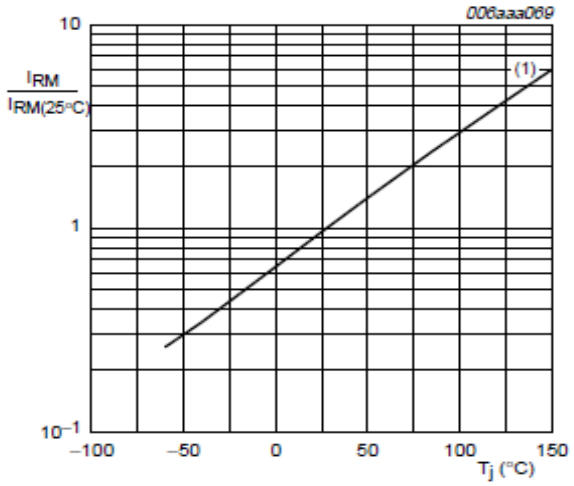
(1) PESD12VL2BT

(2) PESD15VL2BT

(3) PESD24VL2BT

Fig 6. Diode capacitance as a function of reverse voltage; typical values

TYPICAL CHARACTERISTICS



(1) PESD3V3L2BT, PESD5V0L2BT
PESD12VL2BT, PESD15VL2BT and PESD24VL2BT:
I_{RM} < 20 nA; T_j = 150 °C

Fig 7. Relative variation of reverse leakage current as a function of junction temperature; typical values

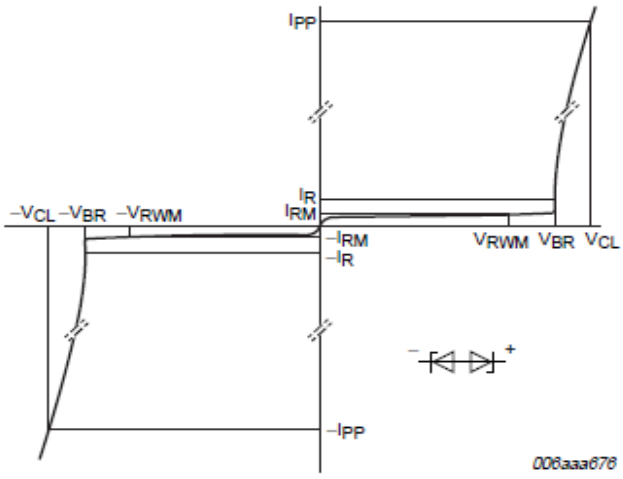


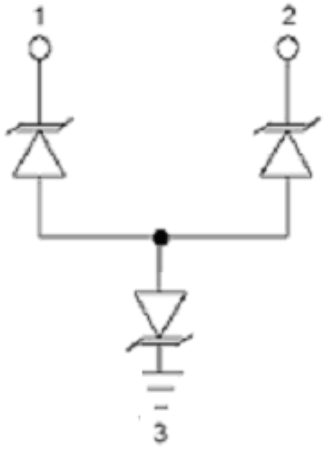
Fig 8. V-I characteristics for a bidirectional ESD protection diode

APPLICATION NOTE

Device Connection for Protection of Two Data Lines

SPE0332 is designed to protect up to two data lines. The bidirection device is connected as follows:

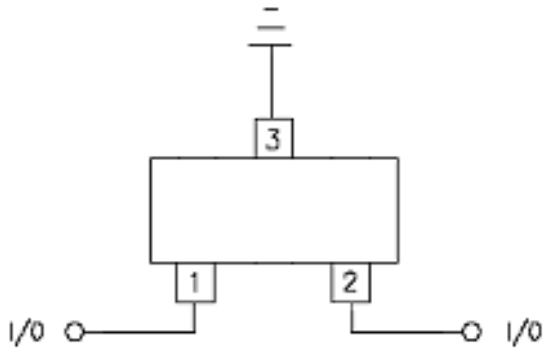
1. The TVS protection of two I/O lines is achieved by connecting pins 1 and 2 to the data lines. Pin 3 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance.



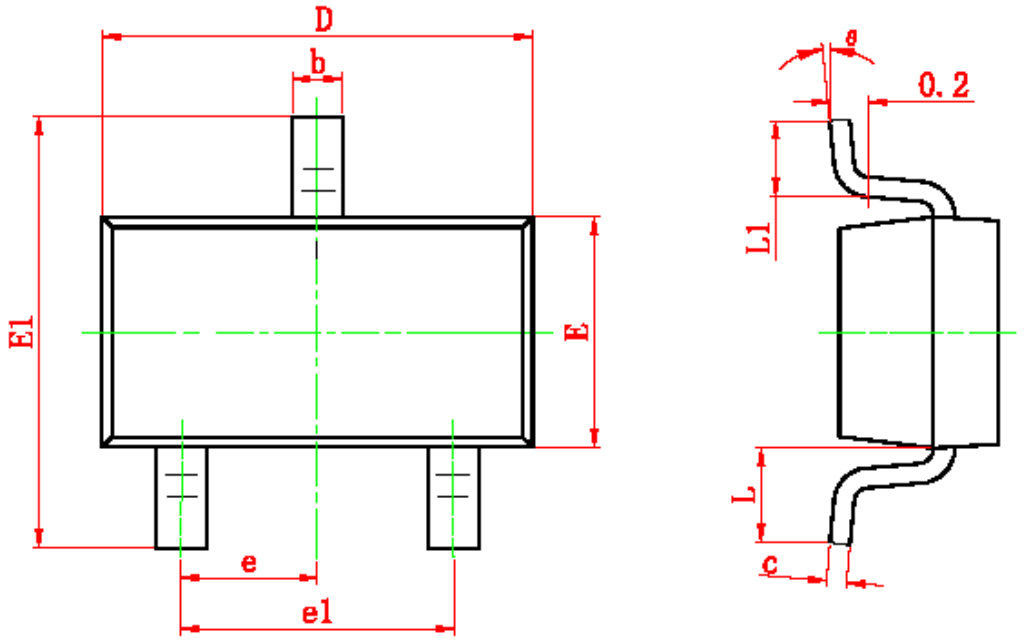
Circuit Board Layout Recommendations for Suppression of ESD

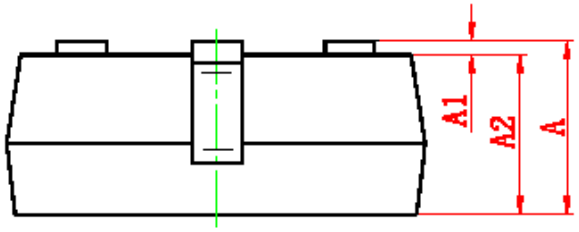
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible.



SOT-23 PACKAGE OUTLINE





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.100	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	6°

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