



SPE1244

3-Line ESD Protection Array

DESCRIPTION

The SPE1244 are designed by TVS array that is to protect sensitive electronics from damage or latch-up due to ESD. They are designed for use in applications where board space is at a premium. SPE1244 will protect up to three line, and may be used on lines where the signal polarities swing above and below ground.

SPE1244 offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

SPE1244 may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small SOT-143 package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

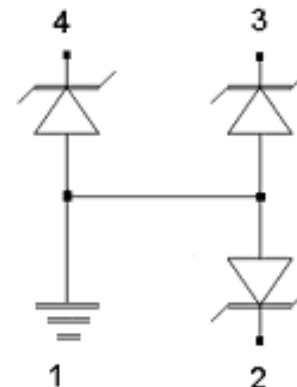
FEATURES

- ◆ Transient protection for data lines to IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact) IEC 61000-4-4 (EFT) 40A (5/50ns)
- ◆ Protects four I/O lines
- ◆ Working voltage: 12V
- ◆ Low leakage current
- ◆ Low operating and clamping voltages

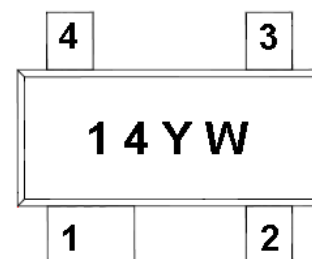
APPLICATIONS

- ◆ ADSL
- ◆ Industrial Electronics
- ◆ RS-422 Interfaces
- ◆ Portable Electronics
- ◆ Microcontroller Input Protection
- ◆ WAN/LAN Equipment

PIN CONFIGURATION (SOT-143-A)



PART MARKING (SOT-143-A)



Y : Year Code
W : Week Code



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ORDERING INFORMATION

Part Number	Package	Part Marking
SPE1244S14ARGB	SOT-143-A	14

※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)

※ SPE1244S14ARGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Peak Pulse Power (tp = 8/20 μs)	Ppk	250	W
Maximum Peak Pulse Current (tp = 8/20 μs)	Ipp	8	A
ESD per IEC 61000 – 4 – 2 (Air)	Vpp	±15	KV
ESD per IEC 61000 – 4 – 2 (Contact)	Vpp	±8	KV
Operating Junction Temperature	Tj	-55 ~ 125	°C
Storage Temperature Range	TSTG	-55 ~ 150	°C
Lead Soldering Temperature	Tl	260 (10sec)	°C

ELECTRICAL CHARACTERISTICS

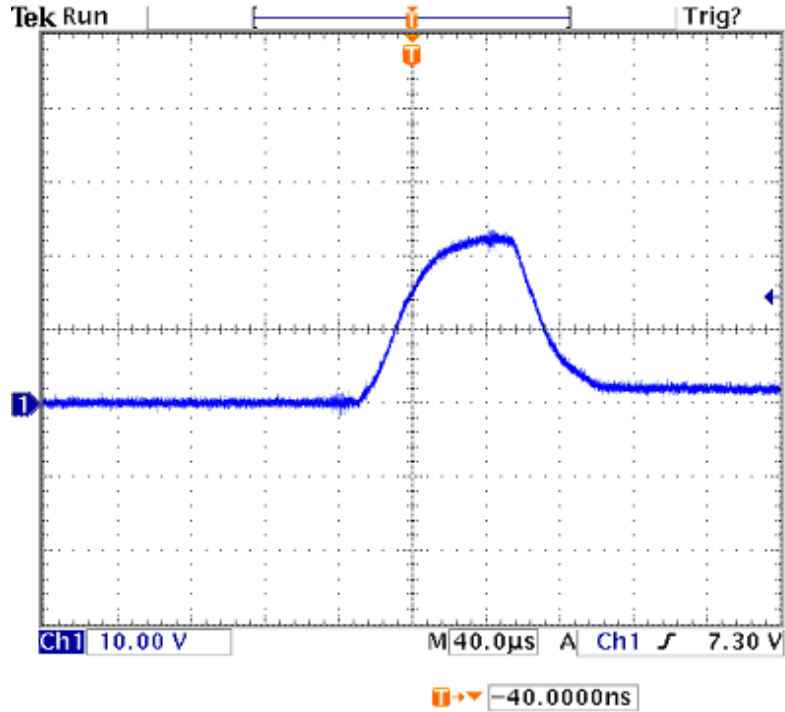
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Reverse Stand – Off Voltage	VRWM				12	V
Reverse Breakdown Voltage	VBR	It = 1mA	13.3			V
Reverse Leakage Current	IR	VRWM = 12V , T=25°C			1	μA
Clamping Voltage	Vc	Ipp = 1A , tp = 8/20 μs			19	V
Clamping Voltage	Vc	Ipp = 8A , tp = 8/20 μs			25	V
Junction Capacitance	Cj	Between I/O Pin and GND VR = 0V , f = 1MHz		16	20	pF

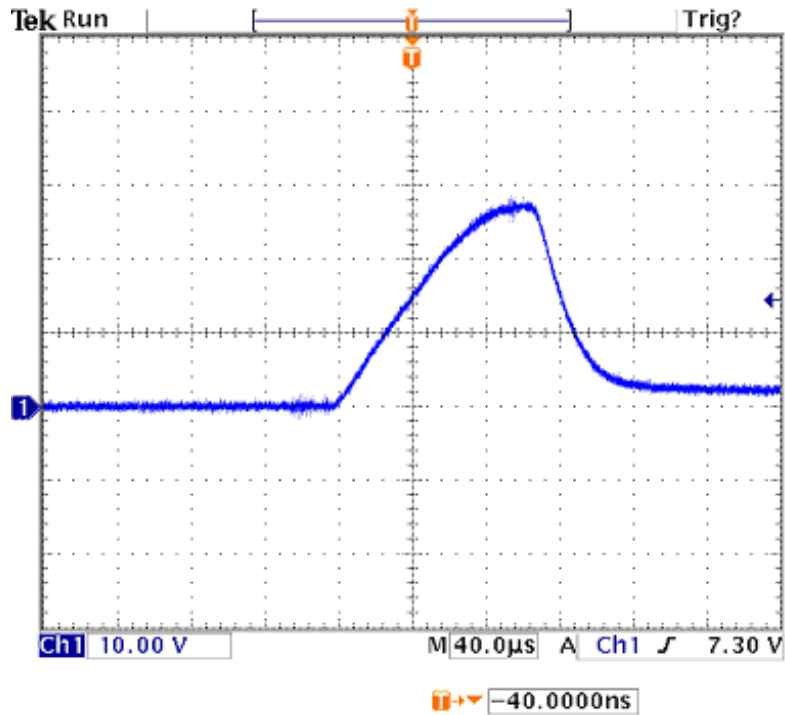


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TYPICAL CHARACTERISTICS



Clamping Voltage ($I_{pp} = 1A$, $t_p = 8/20 \mu s$)



Clamping Voltage ($I_{pp} = 8A$, $t_p = 8/20 \mu s$)



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TYPICAL CHARACTERISTICS

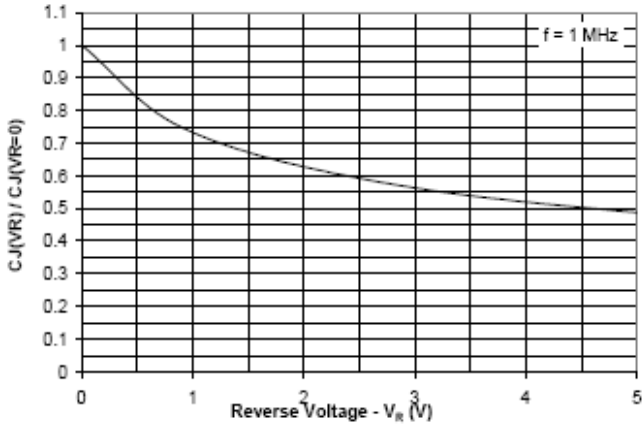


Fig 1 : Junction Capacitance V.S Reverse Voltage Applied

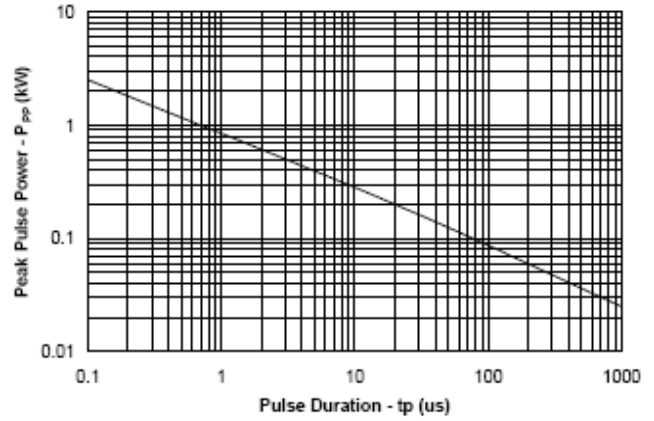


Fig 2 : Peak Plus Power V.S Exponential Plus Duration

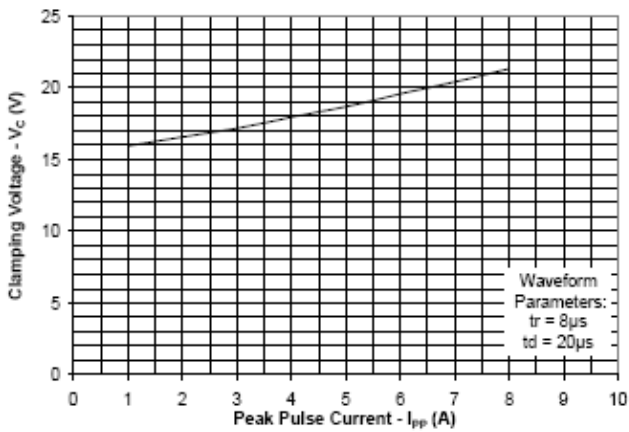


Fig 3 : Clamp Voltage V.S Peak Pulse Current

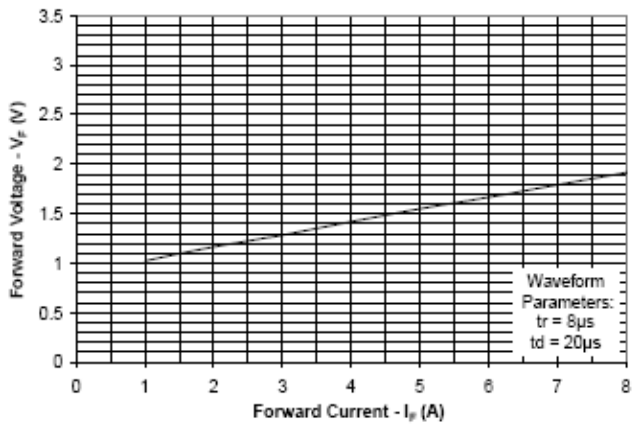


Fig 4 : Forward Voltage Drop V.S Peak Forward



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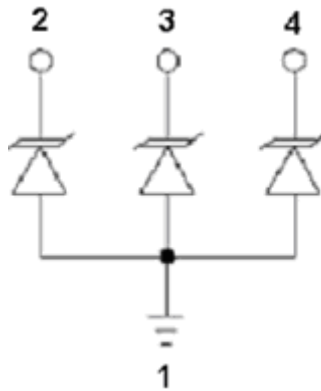
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APPLICATION NOTE

Device Connection for Protection of Four Data Lines

SPE1244 is designed to protect up to three data lines. The device is connected as follows:

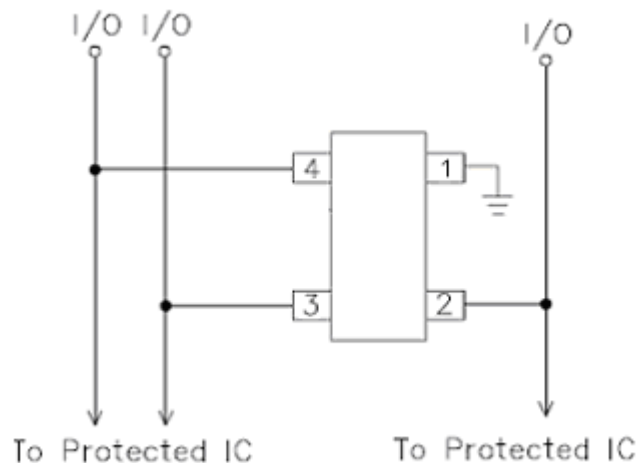
1. The TVS protection of four I/O lines is achieved by connecting pins 1, 2, 4. Pin 3 are connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance.



Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible.





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