



# SPN125T04

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN125T04 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

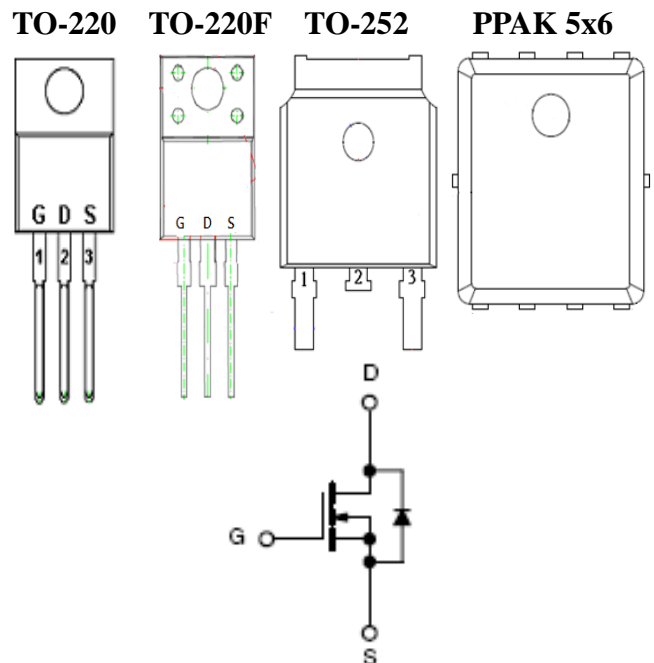
### FEATURES

- ◆ 45V/125A,  $R_{DS(ON)}=4.5m\Omega@V_{GS}=10V$
- ◆ 45V/125A,  $R_{DS(ON)}=7.0m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L/TO-220F-3L/TO-252-2L/PPAK5x6-8L package design

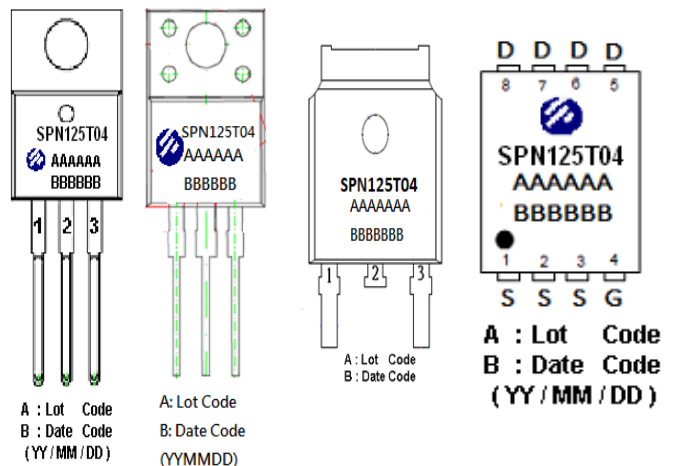
### APPLICATIONS

- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

### PIN CONFIGURATION



### PART MARKING





# SPN125T04

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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

### PPAK5x6 PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN125T04T220TGB	TO-220-3L	SPN125T04
SPN125T04T220FTGB	TO-220F-3L	SPN125T04
SPN125T04T252RGB	TO-252-2L	SPN125T04
SPN125T04DN8RGB	PPAK5x6-8L	SPN125T04

- ※ SPN125T04T220TGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN125T04T220FTGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN125T04T252RGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN125T04DN8RGB : Tape&Reel ; Pb – Free ; Halogen - Free



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### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	45	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current(TJ=150°C) (TO-220/TO-220F/TO-252)	I <sub>D</sub>	Tc=25°C	125	A
		Tc=100°C	88	
Continuous Drain Current(TJ=150°C) (PPAK5x6)	I <sub>D</sub>	Tc=25°C	101	A
		Tc=100°C	64	
Pulsed Drain Current (TO-220/TO-220F/TO-252)	I <sub>DM</sub>	300	A	
Pulsed Drain Current (PPAK5x6)	I <sub>DM</sub>	220	A	
Power Dissipation @ Tc=25°C	P <sub>D</sub>	TO-220	104	W
Power Dissipation @ Tc=25°C		TO252/TO-220F	93	
Power Dissipation @ Tc=25°C		PPAK5x6	83	
Avalanche Energy with Single Pulse ( Tc=25°C, L = 0.1mH. )	E <sub>AS</sub>	141	mJ	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Case (TO-220/TO-220F)	R <sub>θJC</sub>	1.2	°C/W	
Thermal Resistance-Junction to Case (TO-252)	R <sub>θJC</sub>	1.35	°C/W	
Thermal Resistance-Junction to Case (PPAK5X6)	R <sub>θJC</sub>	1.5	°C/W	

#### Note :

- The maximum current rating is package limited at 120A for TO-220-3L
- The maximum current rating is package limited at 78A for TO-220F-3L
- The maximum current rating is package limited at 70A for TO-252-2L
- The maximum current rating is package limited at 80A for PPAK5x6-8L



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	45			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.8	2.2	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=45V, V_{GS}=0V$ $T_J = 25^\circ C$			1	uA
		$V_{DS}=45V, V_{GS}=0V$ $T_J = 100^\circ C$			100	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		3.5	4.5	mΩ
		$V_{GS}=4.5V, I_D=20A$		4.6	7.0	
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=20A$		40		S
Gate Resistance	$R_G$	$V_{GS}=0V, V_{DS}=\text{Open},$ $f=1\text{MHz}$		1.5		Ω
Diode Forward Voltage	$V_{SD}$	$I_F=20A, V_{GS}=0V$		0.9	1.2	V
<b>Dynamic</b>						
Total Gate Charge (10V)	$Q_g$	$V_{DS}=20V, V_{GS}=10V$ $I_D = 20A$		42		nC
Total Gate Charge (4.5V)	$Q_g$			22		
Gate-Source Charge	$Q_{gs}$			4		
Gate-Drain Charge	$Q_{gd}$			10		
Input Capacitance	$C_{iss}$	$V_{DS}=20V, V_{GS}=0V$ $f=1\text{MHz}$		2159		pF
Output Capacitance	$C_{oss}$			756		
Reverse Transfer Capacitance	$C_{rss}$			118		
Turn-On Time	$t_{d(on)}$	$V_{DD}=20V, I_D=20A$ $V_{GEN}=10V, R_G=10\Omega$		12		nS
	$t_r$			10		
Turn-Off Time	$t_{d(off)}$			41		
	$t_f$			16		



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### TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

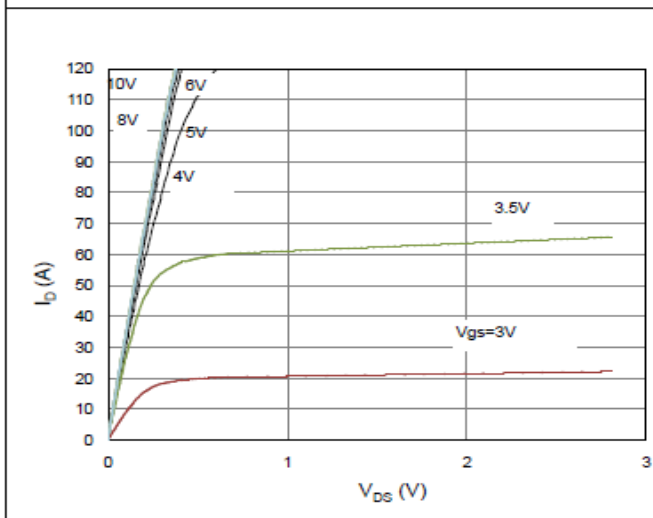


Figure 2. On-Resistance vs. Gate-Source Voltage

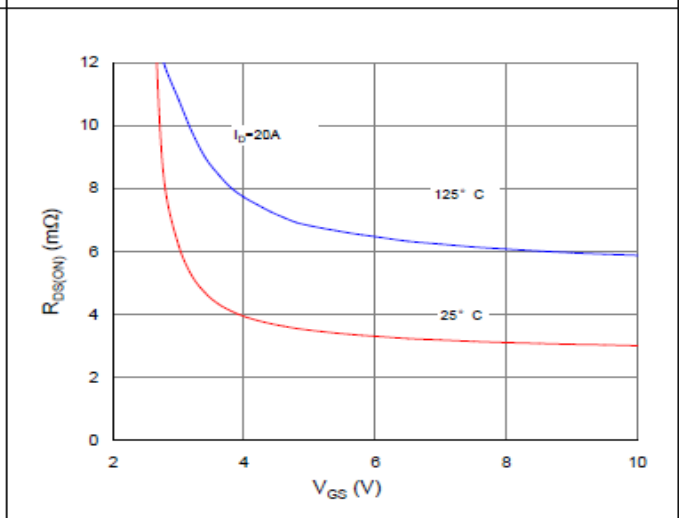


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

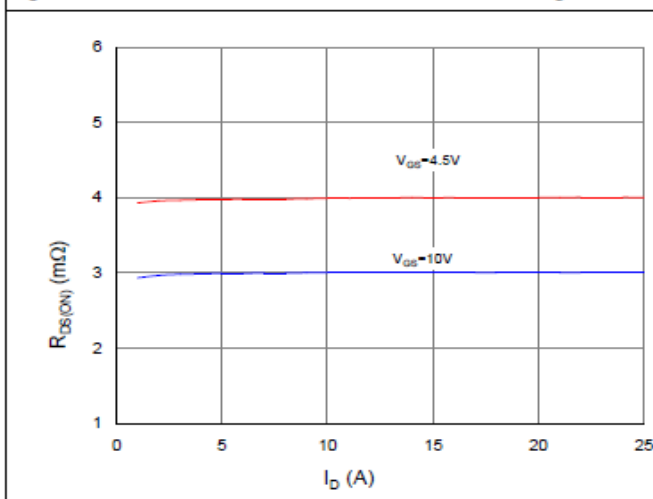


Figure 4. Normalized On-Resistance vs. Junction Temperature

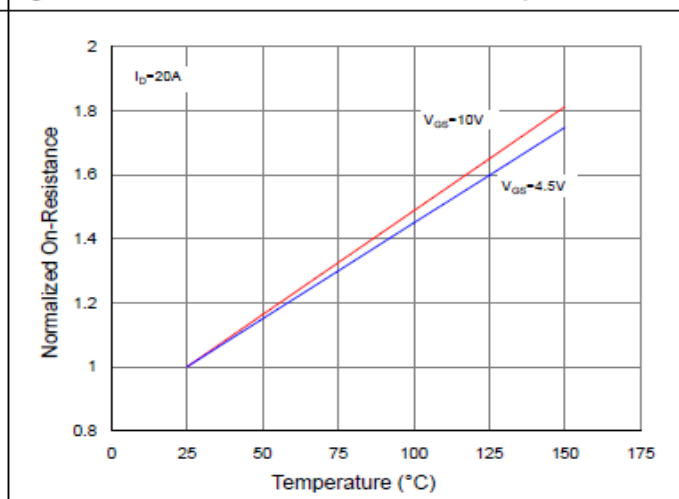


Figure 5. Typical Transfer Characteristics

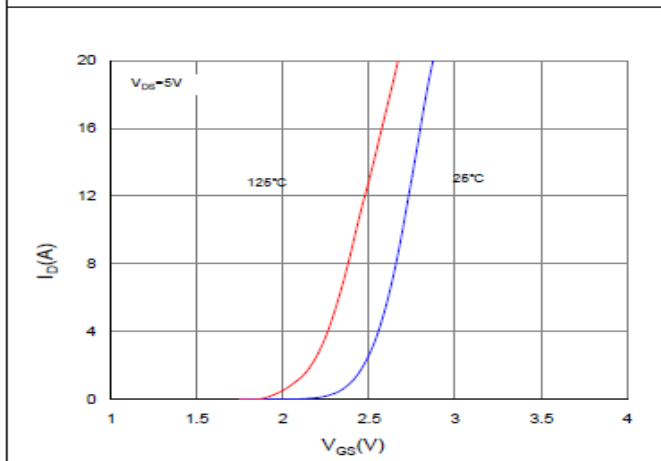
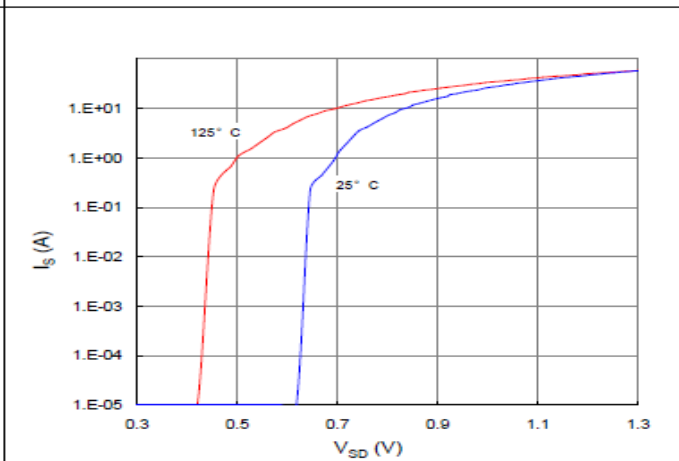


Figure 6. Typical Source-Drain Diode Forward Voltage





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## TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

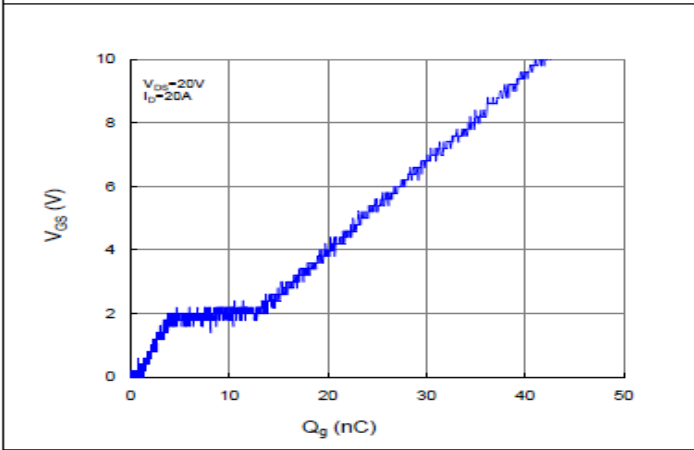


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

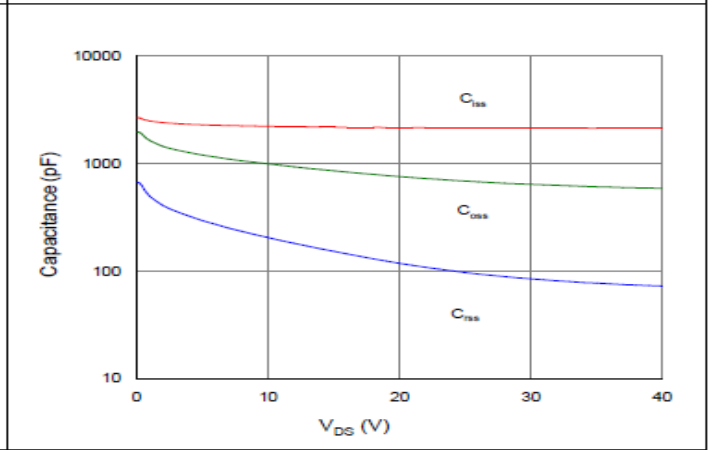


Figure 9. Maximum Safe Operating Area

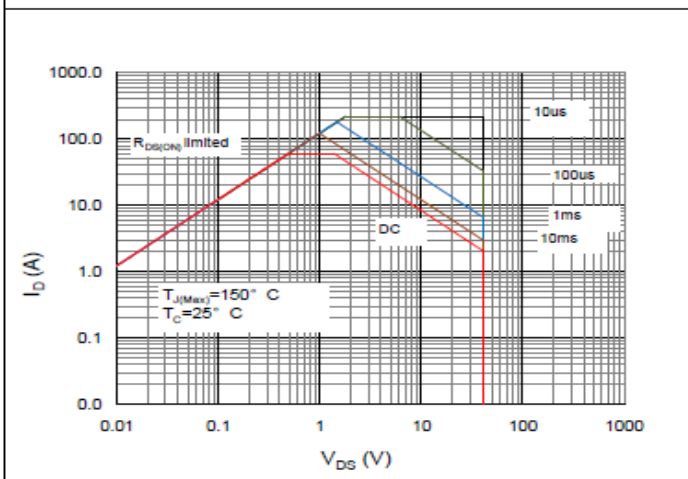


Figure 10. Maximum Drain Current vs. Case Temperature

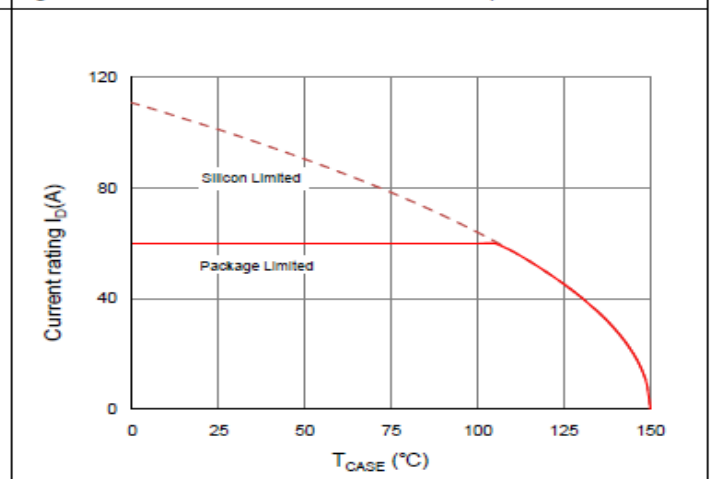
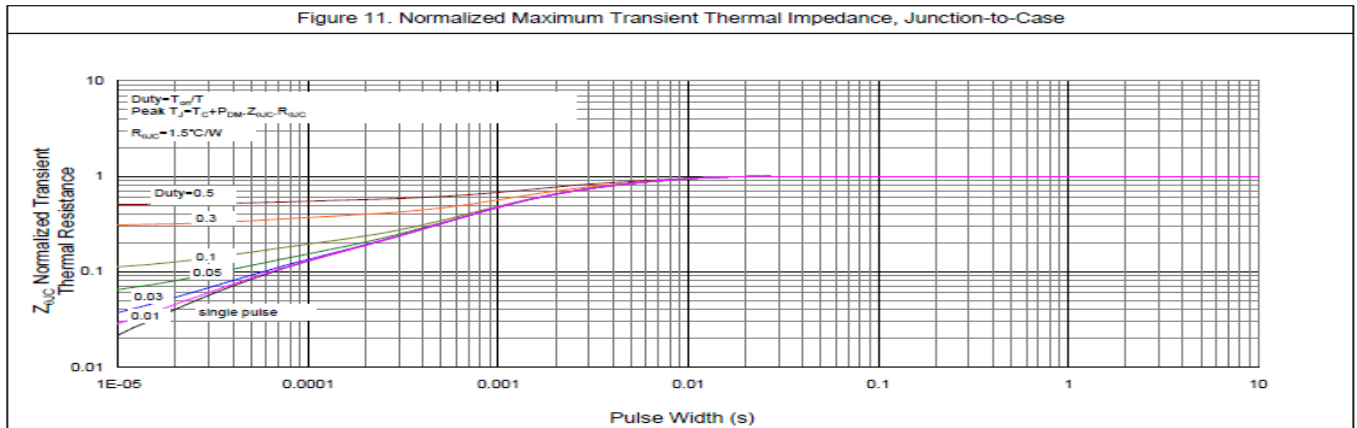


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

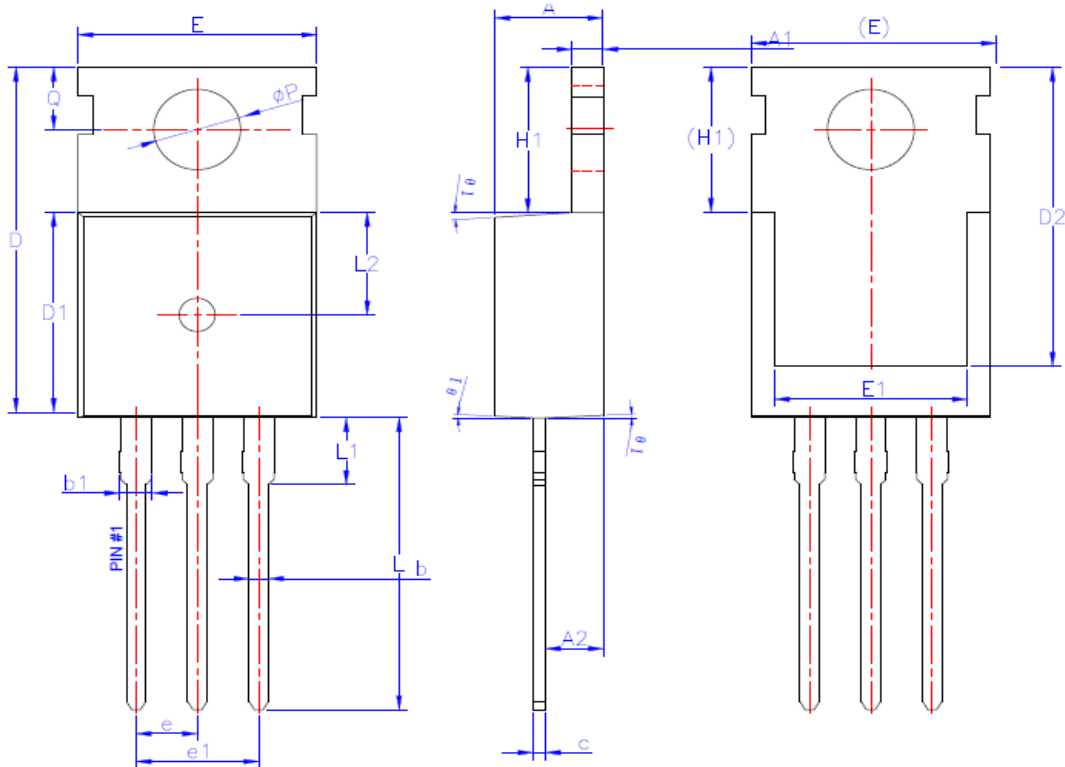




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## N-Channel Enhancement Mode MOSFET

### TO-220-3L PACKAGE OUTLINE



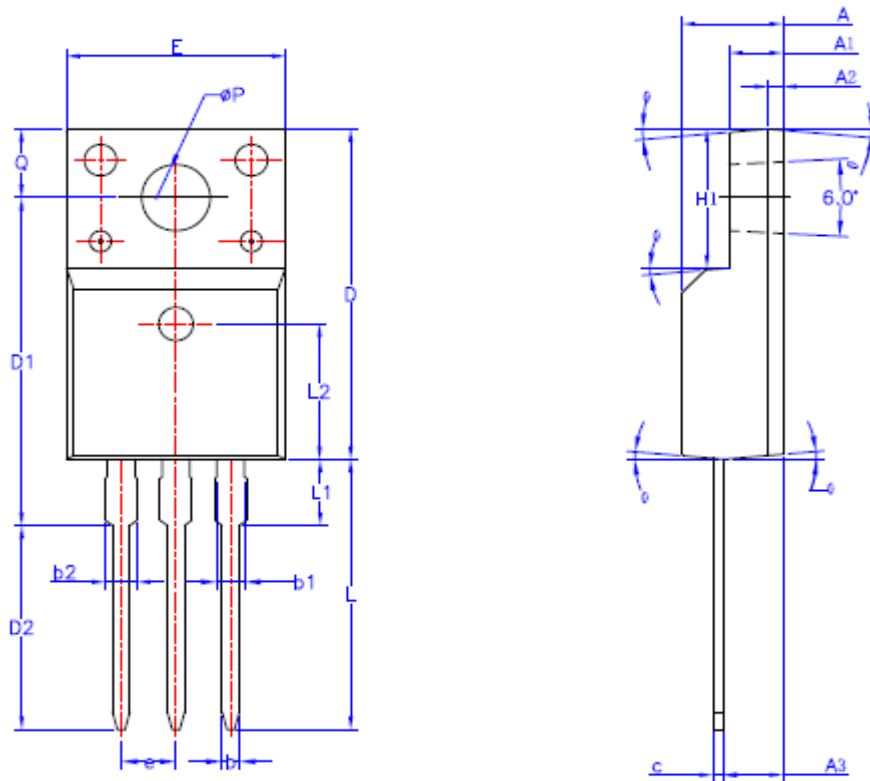
SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	0.60	0.90
b1	-	-	1.40
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	-	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	-	-	3.50
L2	4.6REF		
$\phi P$	3.55	3.60	3.65
Q	2.73	-	2.87
$\theta 1$	1°	3°	5°



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## N-Channel Enhancement Mode MOSFET

### TO-220F-3L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.50	4.70	4.83
A1	2.34	2.54	2.74
A2	0.7REF		
A3	2.56	2.76	2.93
b	0.70	--	0.90
b1	1.18	--	1.40
b2	--	--	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.55	15.75	15.95
D2	9.60	9.80	10.00
E	9.96	10.16	10.36
e	2.54BSC		
H1	6.48	6.68	6.88
L	12.68	12.98	13.28
L1	-	-	3.50
L2	6.50REF		
φ P	3.08	3.18	3.28
Q	3.20	-	3.40
θ 1	1°	3°	5°

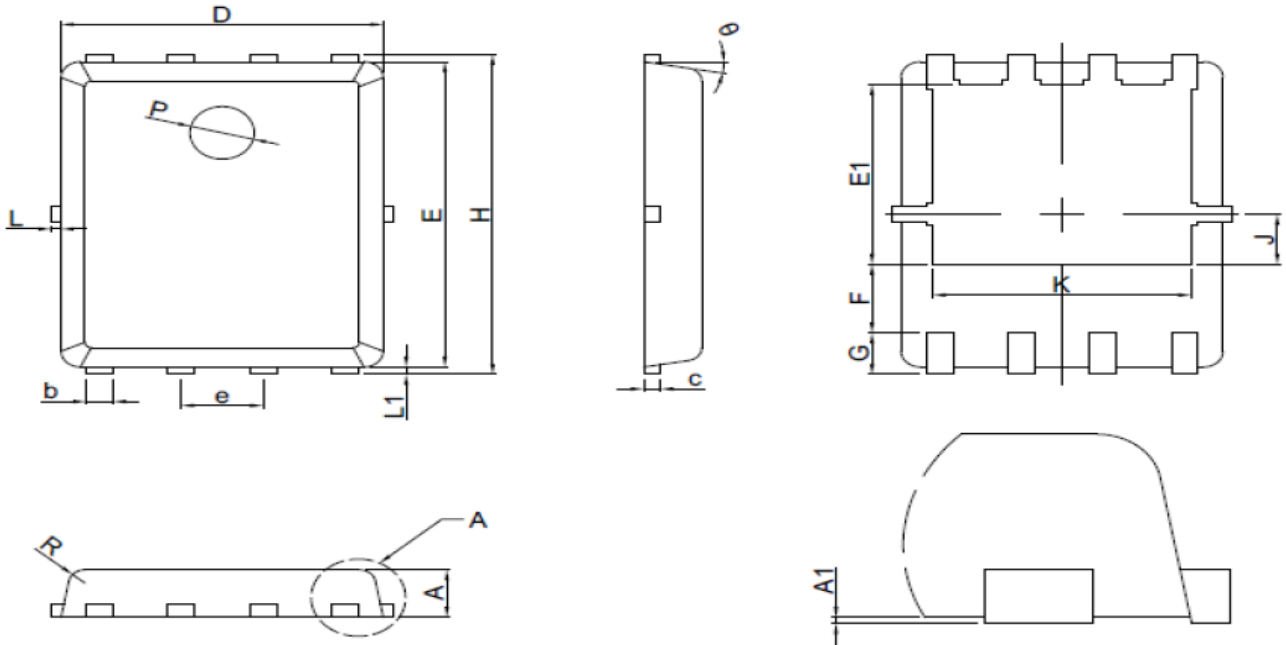




# SPN125T04

## N-Channel Enhancement Mode MOSFET

### PPAK5X6-8L PACKAGE OUTLINE



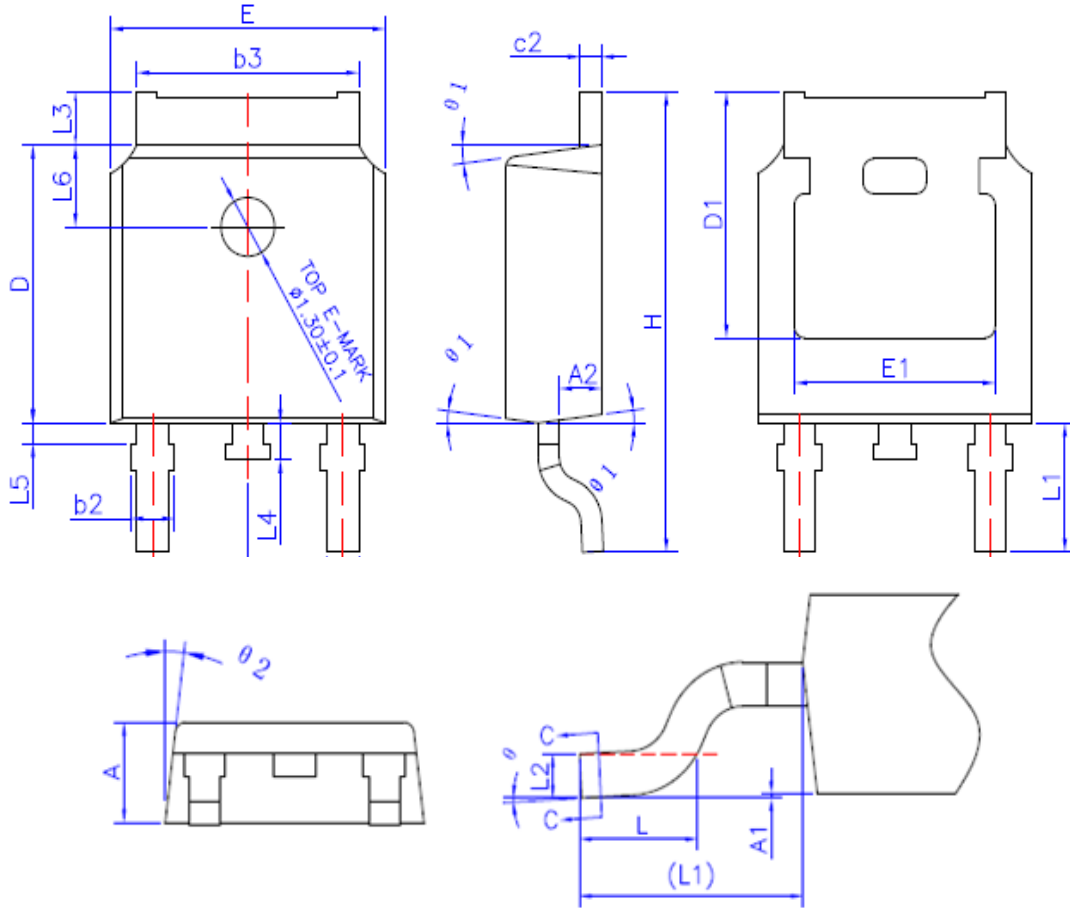
SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.8	0.95	1.1
A1	0.00	0.03	0.05
b	0.33	0.41	0.51
c	0.254 REF		
D	4.80	4.95	5.10
F	1.40 REF		
E	5.70	5.80	5.90
e	1.27 BSC		
H	5.90	6.05	6.20
L1	0.06	0.13	0.20
G	0.60 REF		
J	0.95 BSC		
K	4.00 REF		
L	---	----	0.20
P	1.00 REF		
E1	3.40REF		
E2	0.95 REF		
$\theta$	6°	10°	14°
R	0.25REF		



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### TO-252-2L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	--	0.15
A2	0.90	1.01	1.10
b	0.72	-	0.85
b2	0.72	--	0.90
b3	5.13	5.33	5.46
c	0.47	--	0.60
c2	0.47	--	0.60
D	6.00	6.10	6.20
D1	5.25	--	--
E	6.40	6.60	6.80
E1	4.70	--	--
e	2.3REF		
H	9.80	10.10	10.40
L	1.40	1.60	1.80
L1	2.90REF		
L2	0.508BSC		
L3	0.90	--	1.25
L4	0.60	0.80	1.00
L5	0.15	--	0.75
L6	1.80REF		
$\theta$	0°	3°	8°
$\theta 1$	5°	7°	9°
$\theta 2$	5°	7°	9°



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