SPN1304
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN1304 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

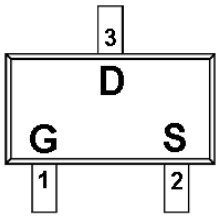
APPLICATIONS

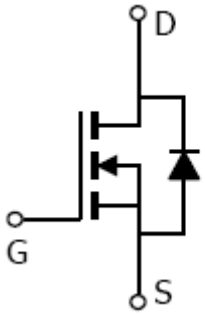
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

FEATURES

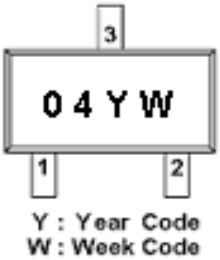
- 20V/2.0A,$R_{DS(ON)}$=225mΩ@V_{GS}=4.5V
- 20V/1.5A,$R_{DS(ON)}$=315mΩ@V_{GS}=2.5V
- 20V/1.0A,$R_{DS(ON)}$=425mΩ@V_{GS}=1.8V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-323 (SC–70) package design

PIN CONFIGURATION (SOT-323 ; SC-70)





PART MARKING



Y : Year Code
W : Week Code

SPN1304
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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN1304S32RGB	SOT-323	04

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPN1304S32RGB : Tape Reel ; Pb – Free, Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate –Source Voltage		V_{GSS}	±12	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	2.0	A
	T_A=70℃		1.5	
Pulsed Drain Current		I_{DM}	10	A
Continuous Source Current(Diode Conduction)		I_S	1.6	A
Power Dissipation	T_A=25℃	P_D	1.25	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	105	℃/W

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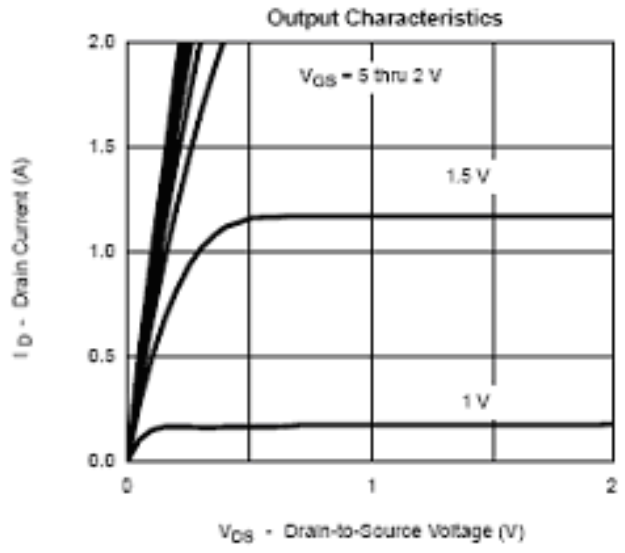
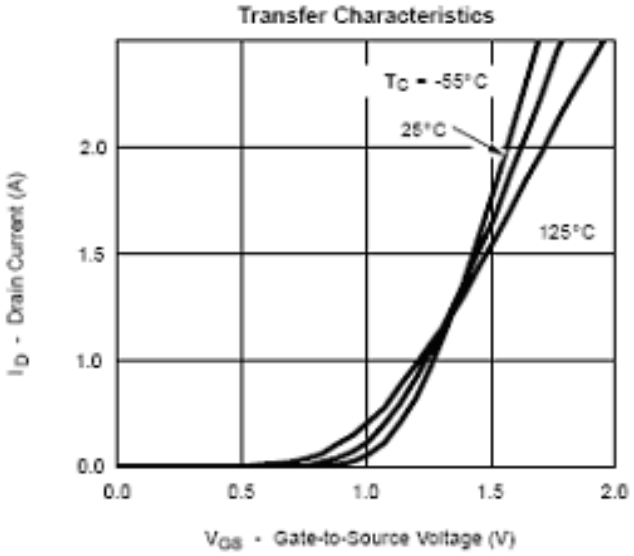
ELECTRICAL CHARACTERISTICS

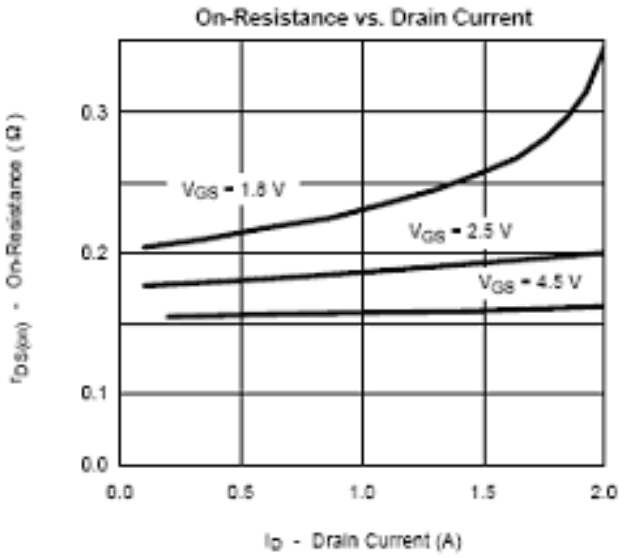
(T_A=25℃ Unless otherwise noted)

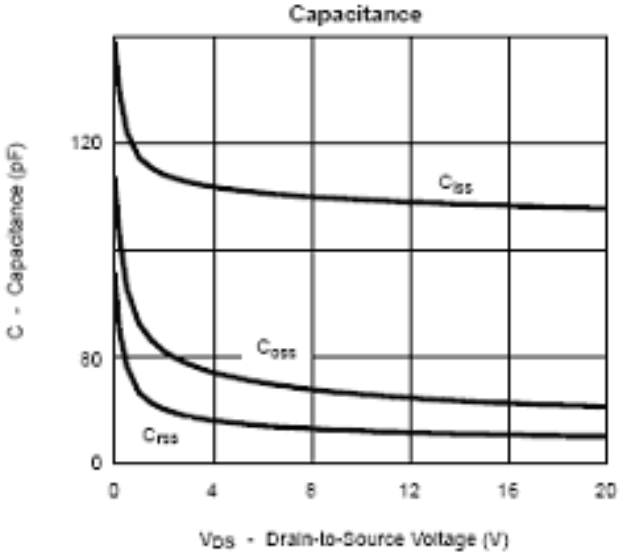
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D= 250uA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	0.35		1.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}= 20V,V_{GS}=0V			1	uA
		V_{DS}= 20V,V_{GS}=0V T_J=55℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥ 4.5V,V_{GS} =5V	2			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=4.5V,I_D=2.0A		0.150	0.225	Ω
		V_{GS}=2.5V,I_D=1.5A		0.210	0.315	
		V_{GS}=1.8V,I_D=1.0A		0.320	0.425	
Forward Transconductance	gfs	V_{DS}=10V,I_D=1.2A		2.6		S
Diode Forward Voltage	V_{SD}	I_S=0.5A,V_{GS}=0V		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=10V,V_{GS}=4.5V, I_D≡0.7A		1.2	1.5	nC
Gate-Source Charge	Q_{gs}			0.2		
Gate-Drain Charge	Q_{gd}			0.3		
Input Capacitance	C_{iss}	V_{DS}=10V_{GS}=0V f=1MHz		45		pF
Output Capacitance	C_{oss}			30		
Reverse Transfer Capacitance	C_{rss}			10		
Turn-On Time	$t_{d(on)}$	V_{DD}=10V,R_L=10Ω , I_D≡1.0A V_{GEN}=4.5V ,R_G=6Ω		5	10	nS
	t_r			8	15	
Turn-Off Time	$t_{d(off)}$			10	18	
	t_f			1.2	2.8	

TYPICAL CHARACTERISTICS









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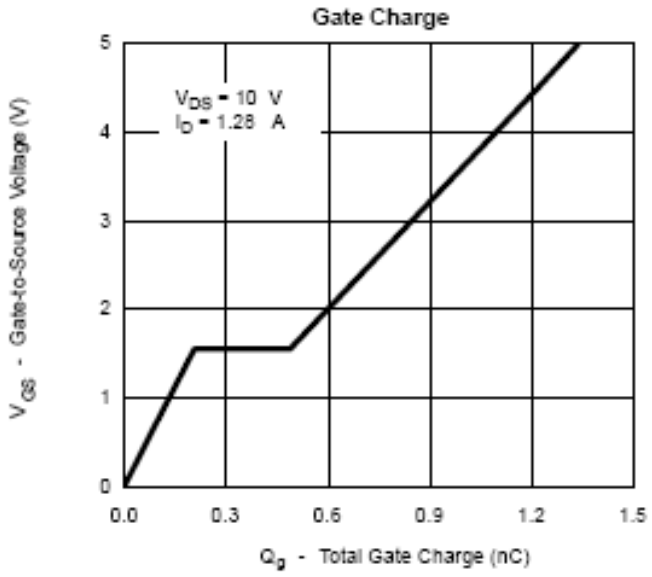

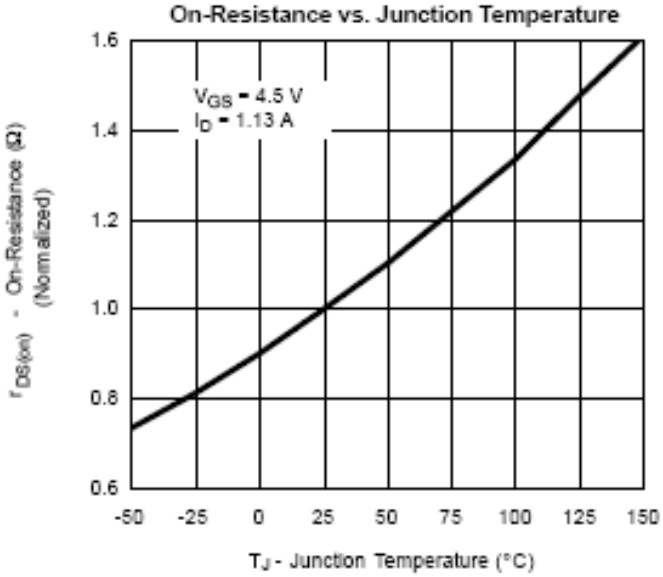

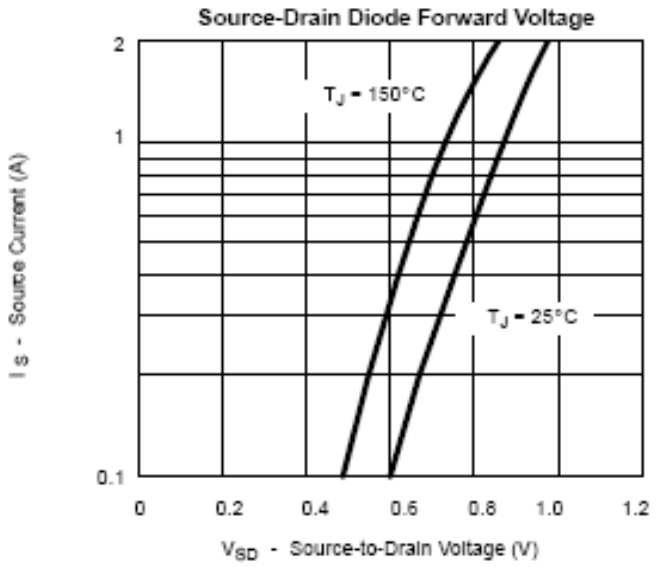

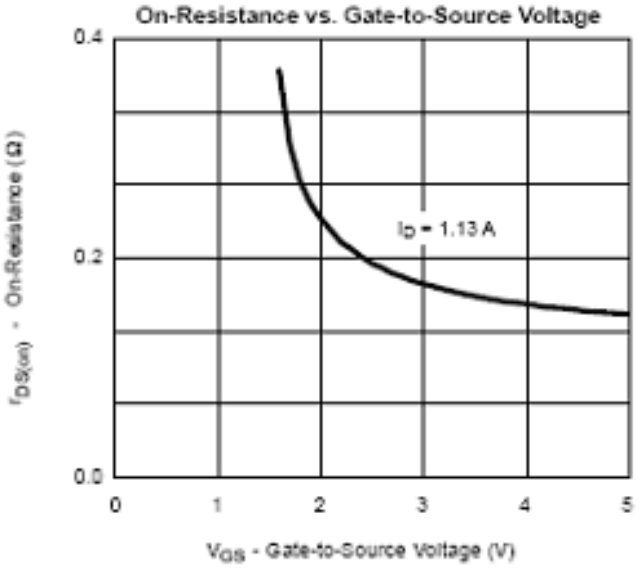

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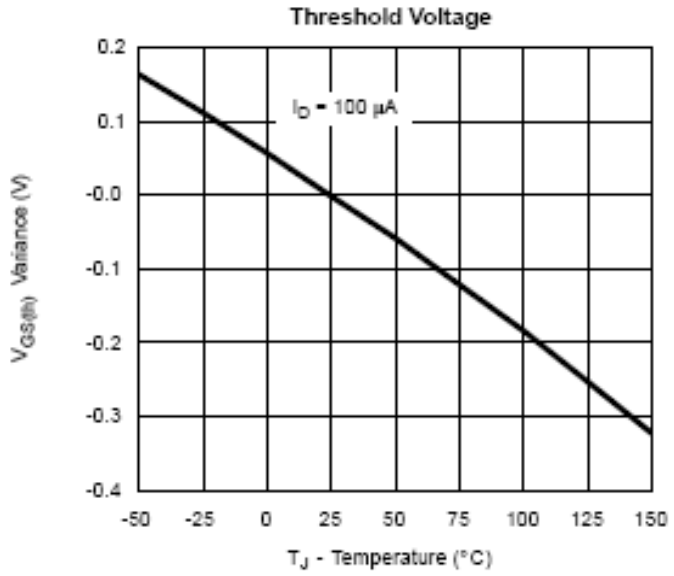

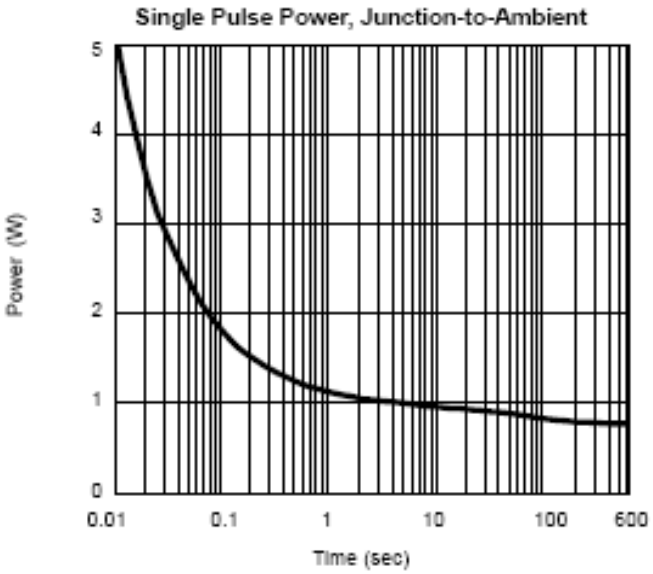

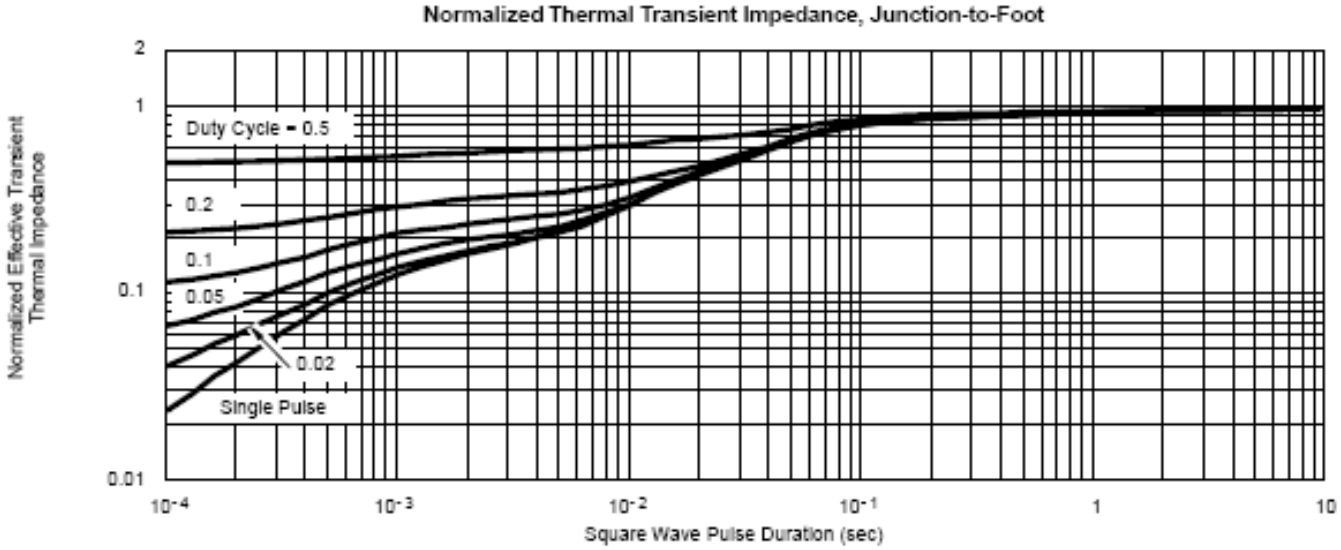

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