



# SPN180T10

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN180T10 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### FEATURES

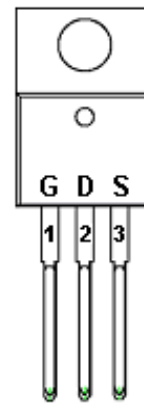
- ◆ 100V/20A,  $R_{DS(ON)}=3.7m\Omega@V_{GS}=10V$
- ◆ High density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L and TO-263-2L package design

### APPLICATIONS

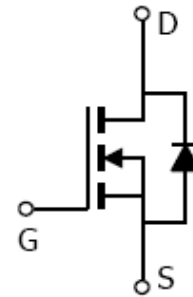
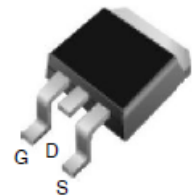
- AC/DC Synchronous Rectifier
- Load Switch
- UPS
- Power Tool
- Motor Control

### PIN CONFIGURATION

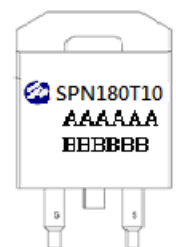
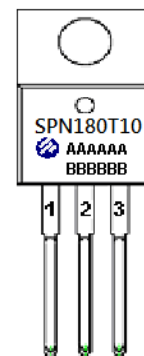
TO-220



TO-263-2L



### PART MARKING



AAAAA: Wafer lot no  
BBBBBB : date code

A : Lot Code  
B : Date Code  
(YY/MM/DD)



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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN180T10T220TGB	TO-220-3L	SPN180T10
SPN180T10T262RGB	TO-263-2L	SPN180T10

※ SPN180T10T220TGB : Tube ; Pb – Free ; Halogen - Free

※ SPN180T10T262RGB : Tape&Reel ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	100	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	180	A
		TA=70°C	135	
Pulsed Drain Current	I <sub>DM</sub>	400	A	
Avalanche Energy, Single Pulse @ L=0.1mH, TA=25°C	E <sub>AS</sub>	180	mJ	
Power Dissipation @ TA=25°C	P <sub>D</sub>	166	W	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	62	°C/W	



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### ELECTRICAL CHARACTERISTICS

(T<sub>A</sub>=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	100			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.0		4.0	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V			1	μA
		V <sub>DS</sub> =100V, V <sub>GS</sub> =0V T <sub>J</sub> =100°C			100	
Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		3.4	3.7	mΩ
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		90		S
Gate Resistance	R <sub>G</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =Open, f=1MHz		0.7		Ω
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V			1.2	V
<b>Dynamic</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =10V I <sub>D</sub> =20A		118		nC
Gate-Source Charge	Q <sub>gs</sub>			27		
Gate-Drain Charge	Q <sub>gd</sub>			21		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V f=1MHz		7300		pF
Output Capacitance	C <sub>oss</sub>			580		
Reverse Transfer Capacitance	C <sub>rss</sub>			18		
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> =50V, V <sub>GS</sub> =10V I <sub>D</sub> =20A, R <sub>G</sub> =10Ω		35		nS
	t <sub>r</sub>			56		
Turn-Off Time	t <sub>d(off)</sub>			92		
	t <sub>f</sub>			26		



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### TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

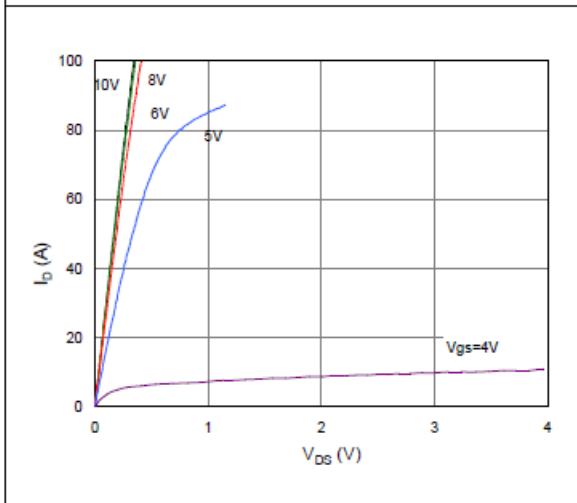


Figure 2. On-Resistance vs. Gate-Source Voltage

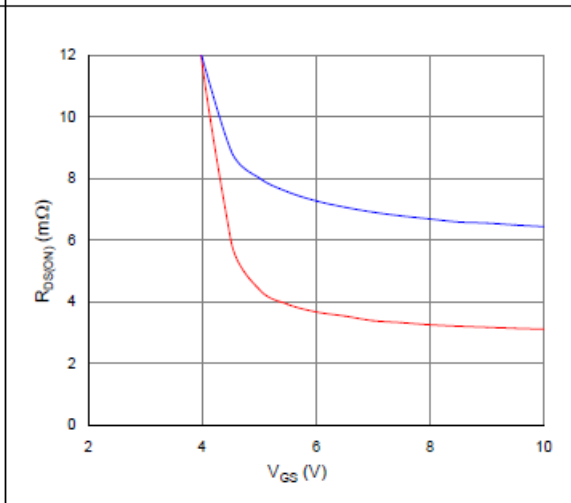


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

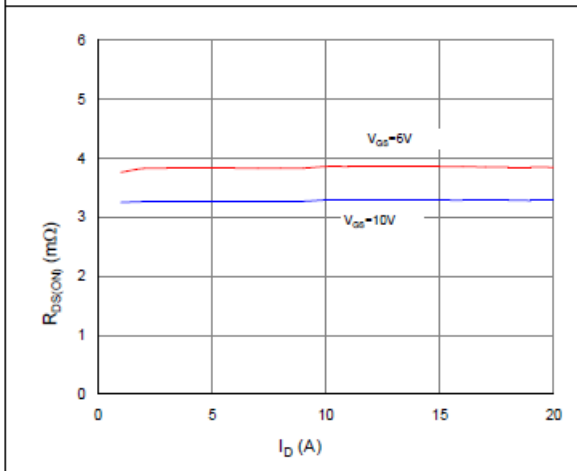


Figure 4. Normalized On-Resistance vs. Junction Temperature

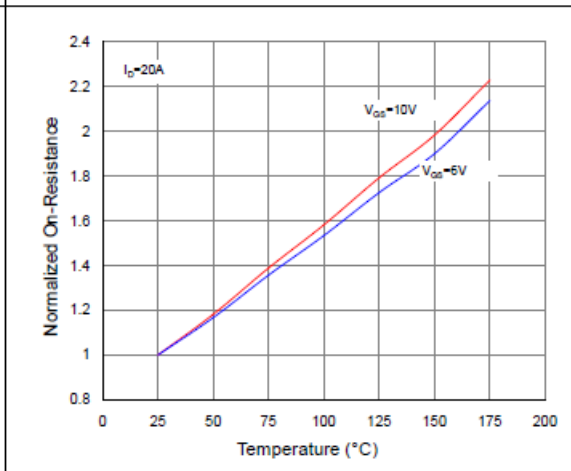


Figure 5. Typical Transfer Characteristics

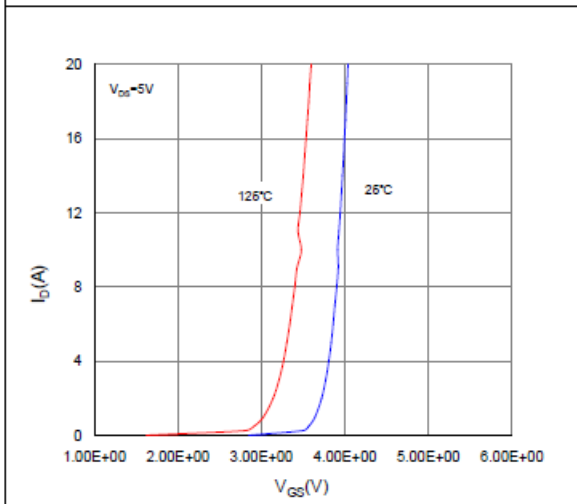
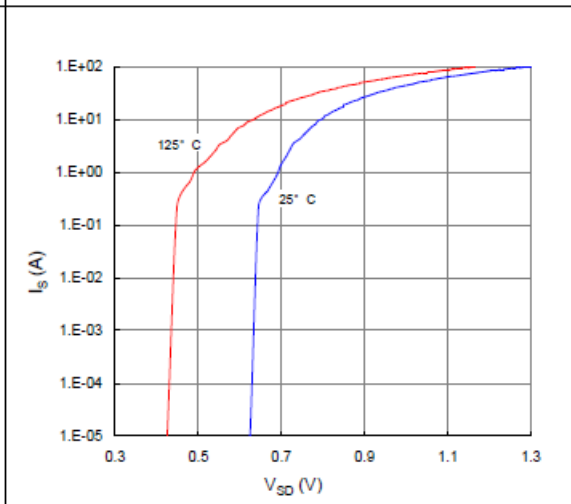


Figure 6. Typical Source-Drain Diode Forward Voltage





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## TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

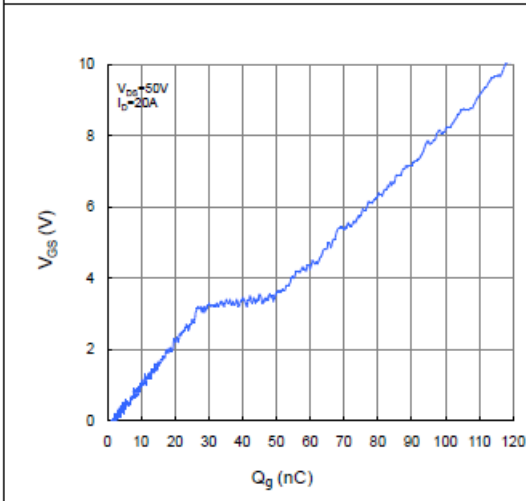


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

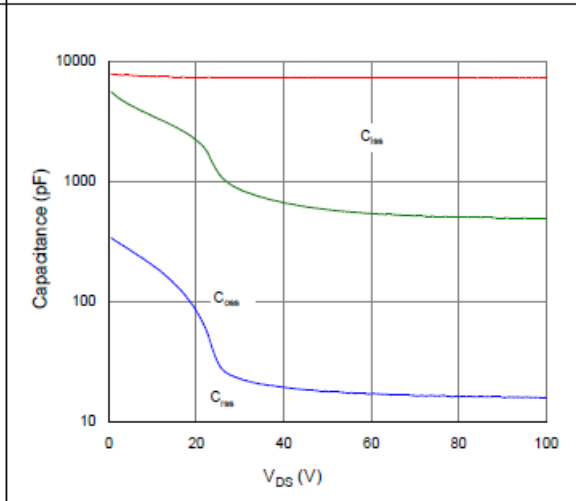


Figure 9. Maximum Safe Operating Area

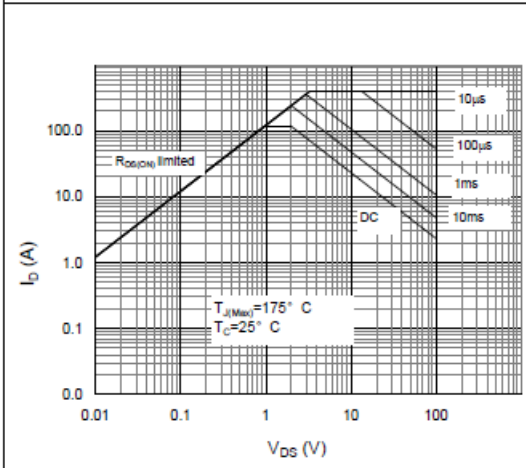


Figure 10. Maximum Drain Current vs. Case Temperature

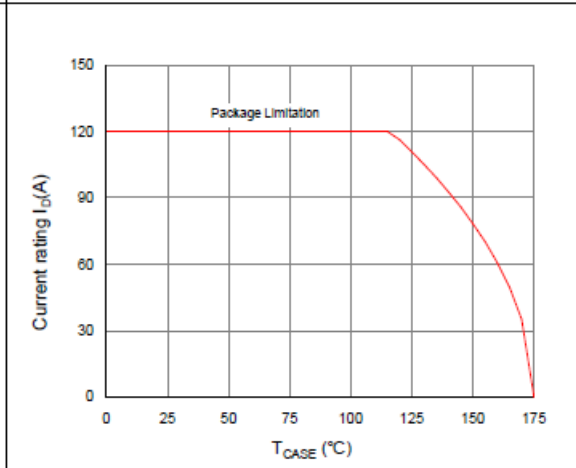
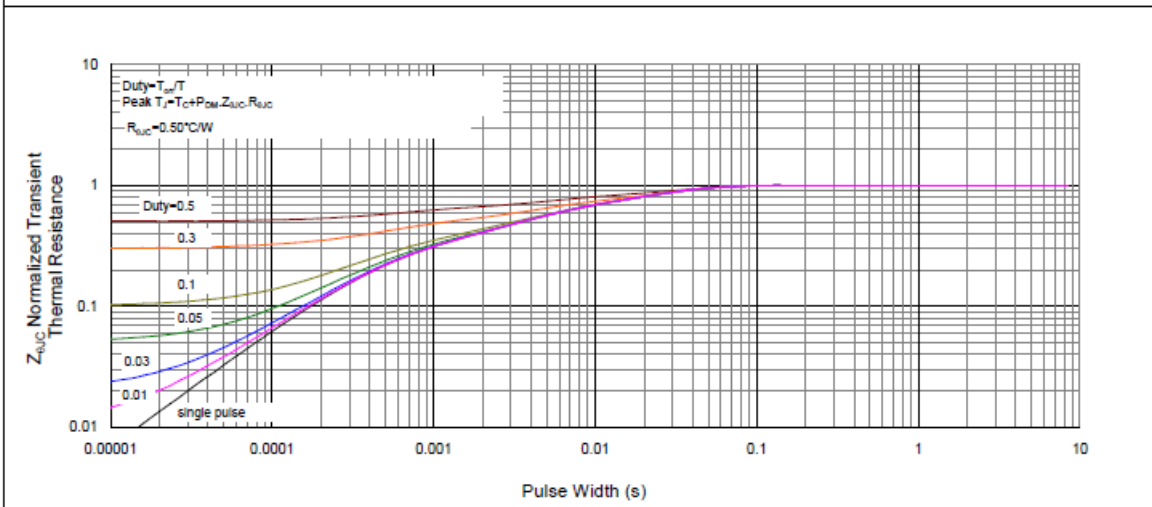


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case





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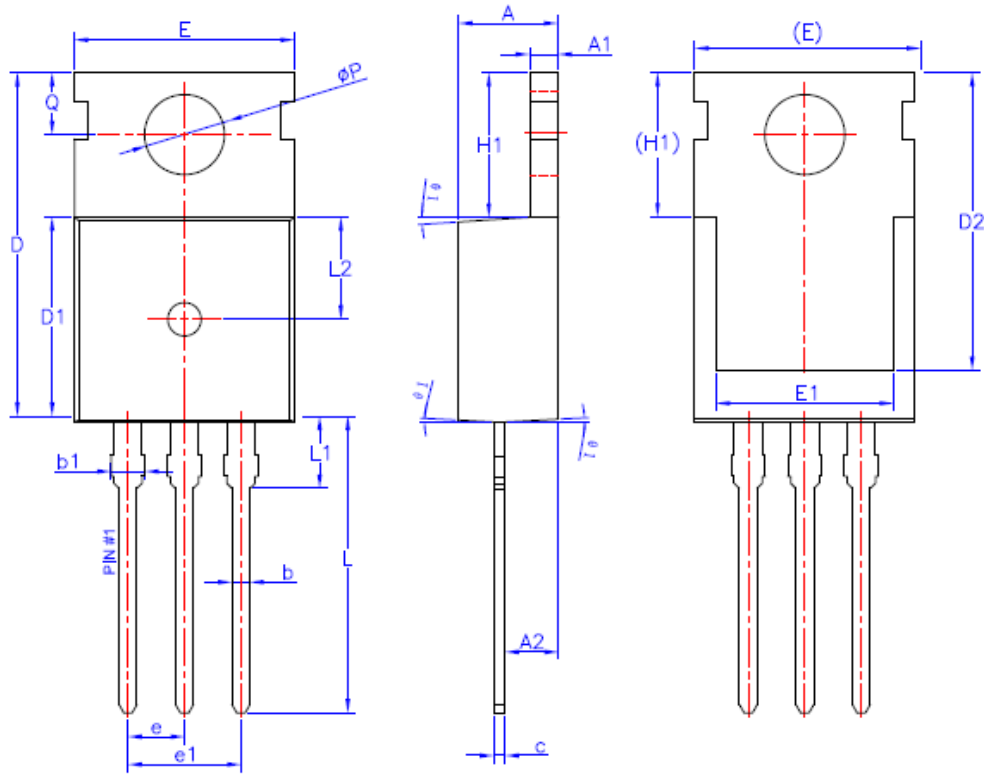
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## N-Channel Enhancement Mode MOSFET

### TO-220 PACKAGE OUTLINE



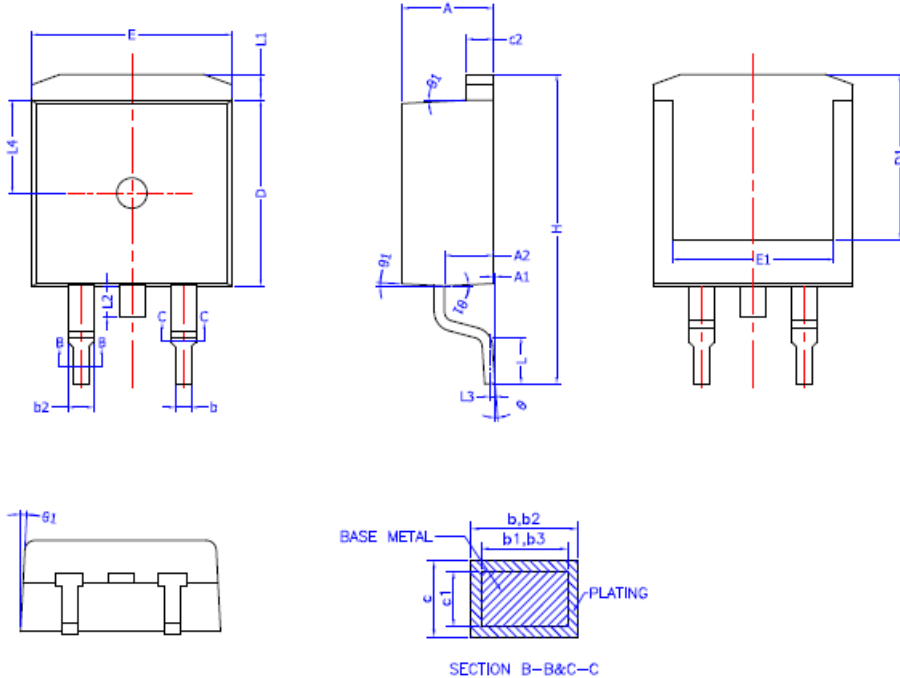
SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	—	0.90
b1	1.42	—	1.57
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	—	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	—	—	3.50
L2	4.60REF		
øP	3.55	3.60	3.65
Q	2.73	—	2.87
θ1	1°	3°	5°



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### TO-263-2L PACKAGE OUTLINE



#### COMMON DIMENSIONS (UNITS OF MEASURE =MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	4,40	4,50	4,60
A1	0	0,10	0,25
A2	2,20	2,40	2,60
b	0,76	—	0,89
b1	0,75	0,80	0,85
b2	1,23	—	1,37
b3	1,22	1,27	1,32
c	0,47	—	0,60
c1	0,46	0,51	0,56
c2	1,25	1,30	1,35
D	9,10	9,20	9,30
D1	8,00	—	—
E	9,80	9,90	10,00
E1	7,80	—	—
e	2,54 BSC		
H	14,90	15,30	15,70
L	2,00	2,30	2,60
L1	1,17	1,27	1,40
L2	—	—	1,75
L3	0,25BSC		
L4	4,60 REF		
$\theta$	0°	—	8°
$\theta_1$	1°	3°	5°

NOTES:  
ALL DIMENSIONS REFER TO JEDEC STANDARD TO-263 AB  
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.





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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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