



# SPN200N04

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN200N04 is the N-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN200N04 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### APPLICATIONS

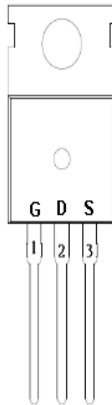
- High Frequency Synchronous Buck Converter
- DC/DC Power System
- Load Switch

### FEATURES

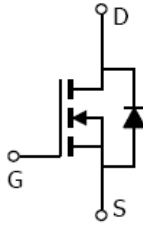
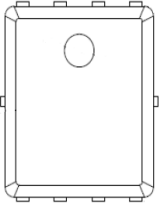
- ◆ 40V/200A,  $R_{DS(ON)}=1.5m\Omega@V_{GS}=10V$  for PPAK5x6
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220 and PPAK5x6-8L package design

### PIN CONFIGURATION

TO-220



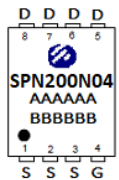
PPAK5x6-8



### PART MARKING



A : Lot Code  
B : Date Code



A : Lot Code  
B : Date Code  
(YY/MM/DD)



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### PIN DESCRIPTION

#### TO-220

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

#### PPAK5x6-8

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN200N04T220TGB	TO-220	SPN200N04
SPN200N04DN8RGB	PPAK5x6-8L	SPN200N04

※ SPN200N04T220TGB : Tube ; Pb – Free ; Halogen - Free

※ SPN200N04DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free



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### ABSOLUTE MAXIMUM RATINGS

( $T_A=25^{\circ}\text{C}$  Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	$V_{DSS}$	40	V	
Gate -Source Voltage	$V_{GSS}$	$\pm 20$	V	
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C=25^{\circ}\text{C}$	200	A
		$T_C=100^{\circ}\text{C}$	120	
Pulsed Drain Current	$I_{DM}$	400	A	
Avalanche Current	$I_{AS}$	116	A	
Single Pulse Avalanche Energy	EAS	673	mJ	
Power Dissipation@ $T_C=25^{\circ}\text{C}$	$P_D$	TO-220	104	W
		PPAK5x6	83	
Operating Junction Temperature	$T_J$	-55/150	$^{\circ}\text{C}$	
Storage Temperature Range	$T_{STG}$	-55/150	$^{\circ}\text{C}$	
Thermal Resistance-Junction to Case	$R_{\theta JC}$	TO-220	1.2	$^{\circ}\text{C}/\text{W}$
		PPAK5x6	1.5	
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	TO-220	62	$^{\circ}\text{C}/\text{W}$
		PPAK5x6	55	



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	2.8	4.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=32V, V_{GS}=0V$			1	uA
		$V_{DS}=32V, V_{GS}=0V, T_J=55^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$			100	A
Drain-Source On-Resistance, TO220	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		1.6	1.9	mΩ
Drain-Source On-Resistance, PPAK5x6				1.3	1.5	
Gate Resistance	$R_g$	$V_{DS}=V_{GS}=0V, f=1MHz$		1.2		Ω
Diode Forward Voltage	$V_{SD}$	$I_S=1A, V_{GS}=0V$			1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=20V, V_{GS}=10V$ $I_D=20A$		108		nC
Gate-Source Charge	$Q_{gs}$			25.4		
Gate-Drain Charge	$Q_{gd}$			26.8		
Input Capacitance	$C_{iss}$	$V_{DS}=20V, V_{GS}=0V$ $f=1MHz$		6601		pF
Output Capacitance	$C_{oss}$			2073		
Reverse Transfer Capacitance	$C_{rss}$			248		
Turn-On Time	$t_{d(on)}$	$V_{DD}=20V,$ $I_D=20A, V_{GEN}=10V$ $R_G=1.5\Omega$		20		nS
	$t_r$			145		
Turn-Off Time	$t_{d(off)}$			55		
	$t_f$			18		



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## TYPICAL CHARACTERISTICS

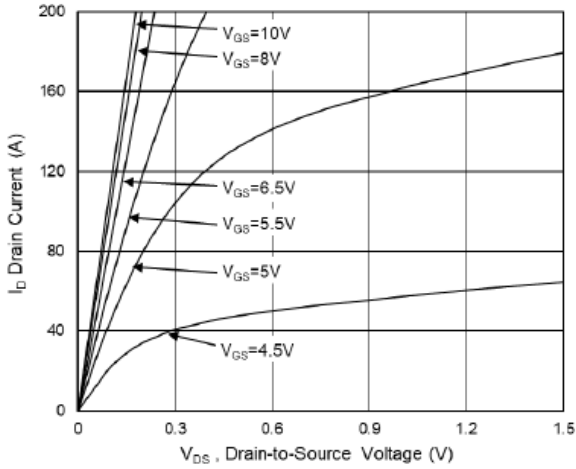


Fig.1 Typical Output Characteristics

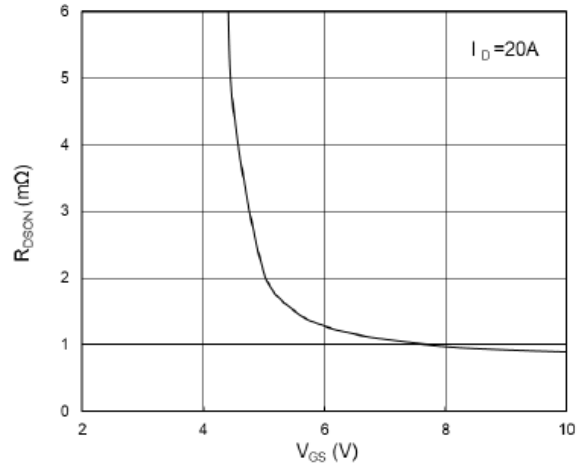


Fig.2 On-Resistance vs G-S Voltage

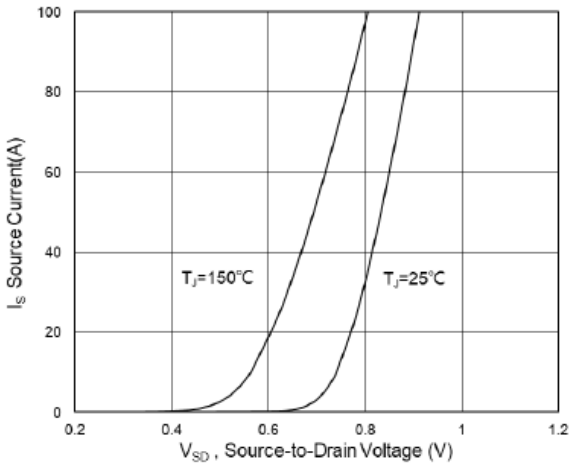


Fig.3 Source Drain Forward Characteristics

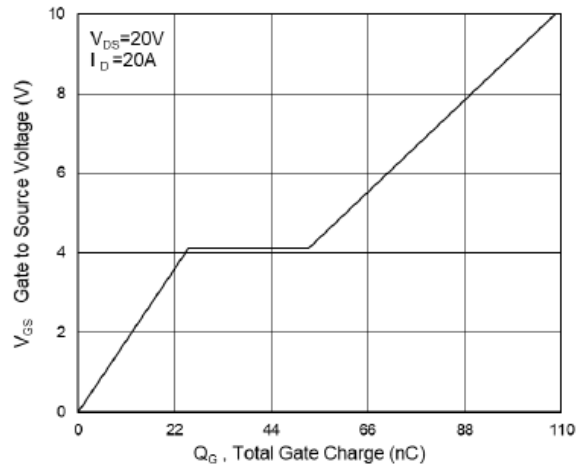


Fig.4 Gate-Charge Characteristics

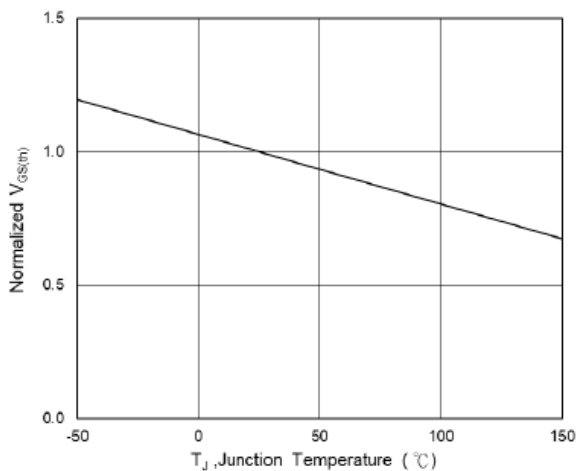


Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$

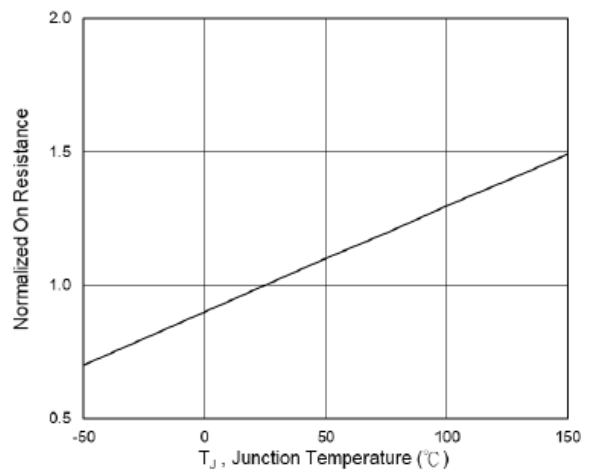


Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$



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## TYPICAL CHARACTERISTICS

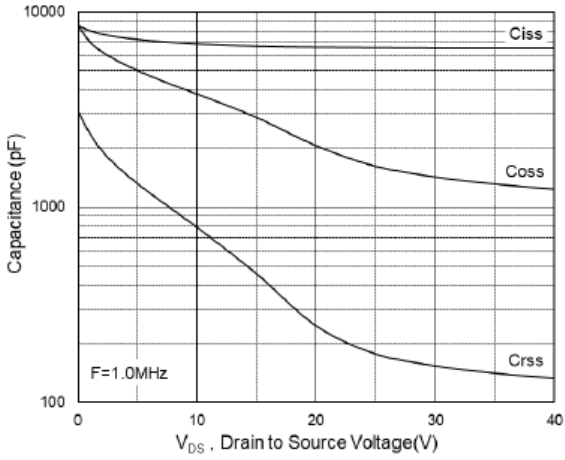


Fig.7 Capacitance

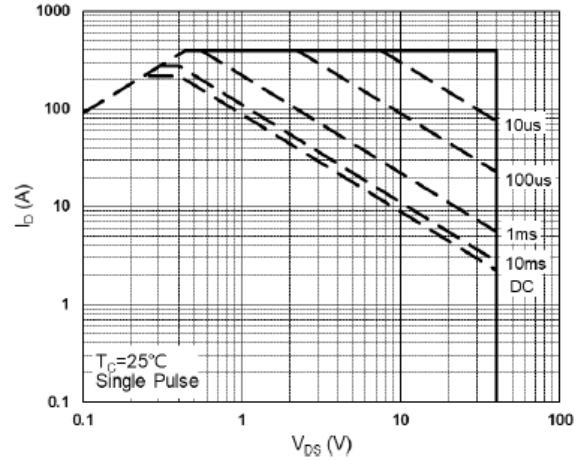


Fig.8 Safe Operating Area

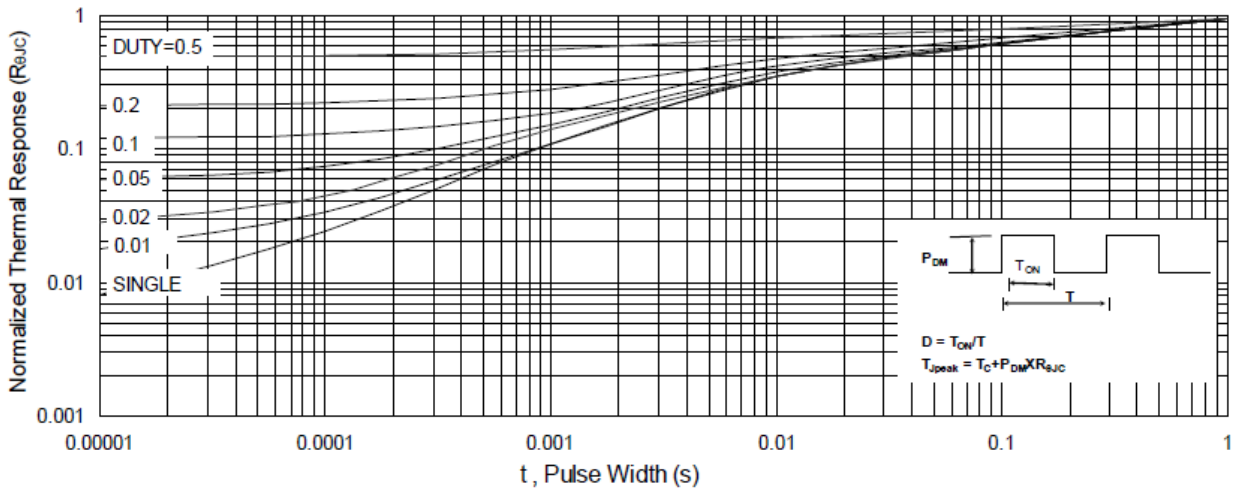


Fig.9 Normalized Maximum Transient Thermal Impedance

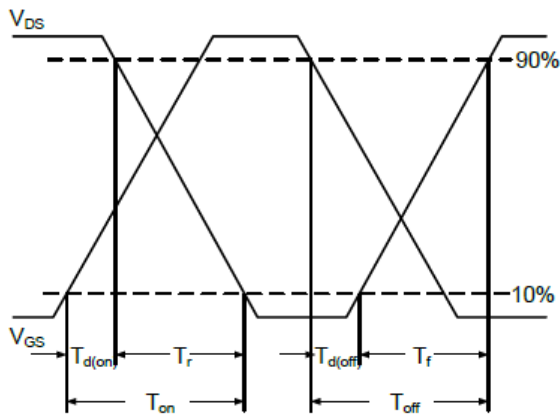


Fig.10 Switching Time Waveform

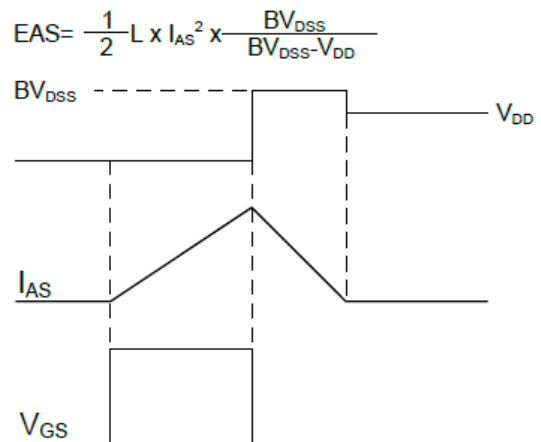


Fig.11 Unclamped Inductive Switching Waveform



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