



SPN2038

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN2038 is the N-Channel logic enhancement mode power field effect transistor which is produced with high cell density DMOS trench technology. The SPN2038 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

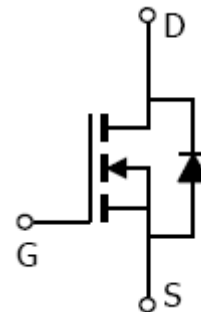
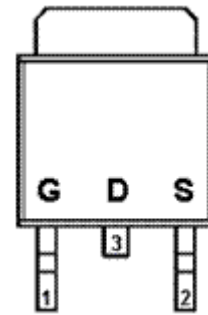
- ◆ 20V/14A, $R_{DS(ON)}=16m\Omega@V_{GS}=4.5V$
- ◆ 20V/7A, $R_{DS(ON)}=22m\Omega@V_{GS}=2.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

TO-252



PART MARKING





SPN2038

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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN2038T252RGB	TO-252	SPN2038

※ SPN2038T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	20	V	
Gate –Source Voltage	V _{GSS}	±16	V	
Continuous Drain Current	I _D	T _C =25°C	28	A
		T _C =100°C	18	
Pulsed Drain Current	I _{DM}	70	A	
Power Dissipation	P _D	T _C =25°C 25	W	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Case	R _{θJC}	5	°C/W	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5		1.2	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 16V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=16V, V_{GS}=0V$			1	uA
		$V_{DS}=16V, V_{GS}=0V$ $T_J=55^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=4.5V$	28			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=14A$		0.016	0.02	Ω
		$V_{GS}=2.5V, I_D=7A$		0.022	0.028	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=14A$		30		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=4.5V$ $I_D=14A$		9.8		nC
Gate-Source Charge	Q_{gs}			2.1		
Gate-Drain Charge	Q_{gd}			3		
Input Capacitance	C_{iss}	$V_{DS}=15, V_{GS}=0V$ $f=1MHz$		772		pF
Output Capacitance	C_{oss}			83		
Reverse Transfer Capacitance	C_{rss}			79		
Turn-On Time	$t_{d(on)}$	$V_{DD}=10V, I_D=14A,$ $V_{GS}=4.5V, R_G=3.3\Omega$		4		nS
	t_r			12.5		
Turn-Off Time	$t_{d(off)}$			20		
	t_f			8		



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TYPICAL CHARACTERISTICS

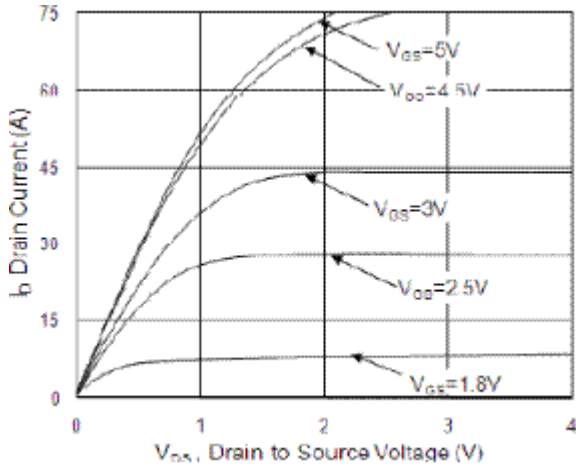


Fig. 1 Typical Output Characteristics

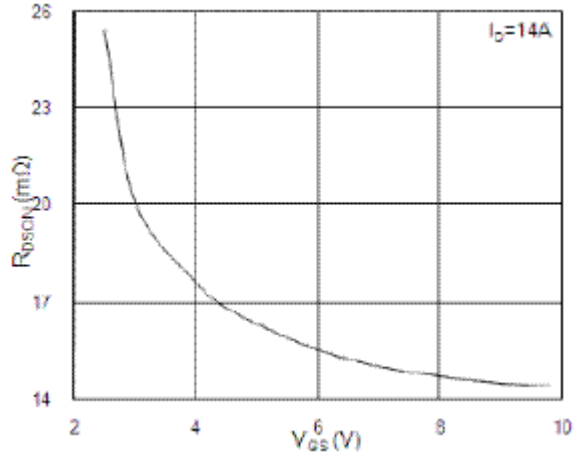


Fig. 2 On-Resistance vs Gate Voltage

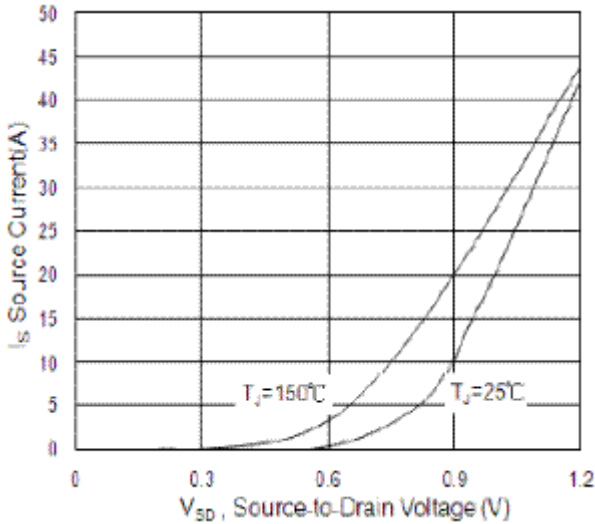


Fig. 3 Forward Characteristics

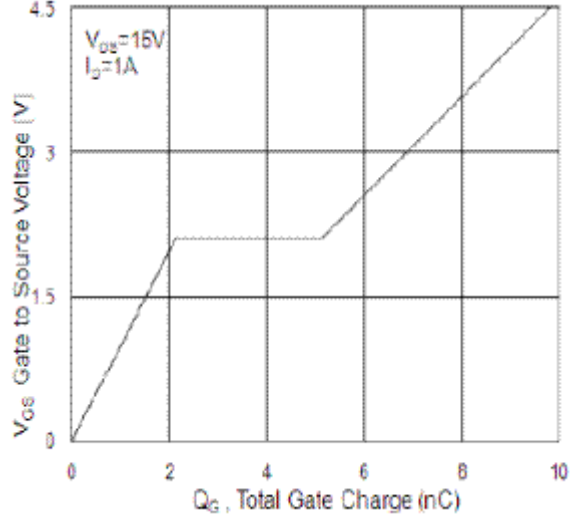


Fig. 4 Total Gate Charge

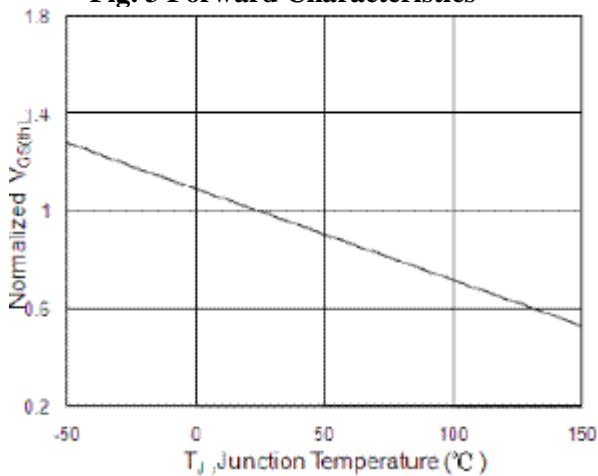


Fig. 5 Vgs vs Temperature

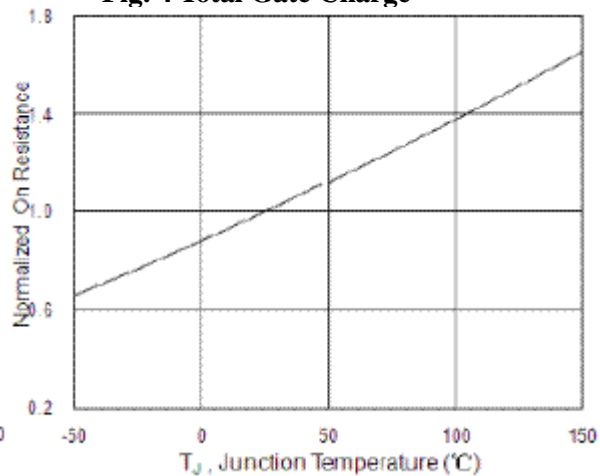


Fig. 6 Rds(on) vs Temperature



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TYPICAL CHARACTERISTICS

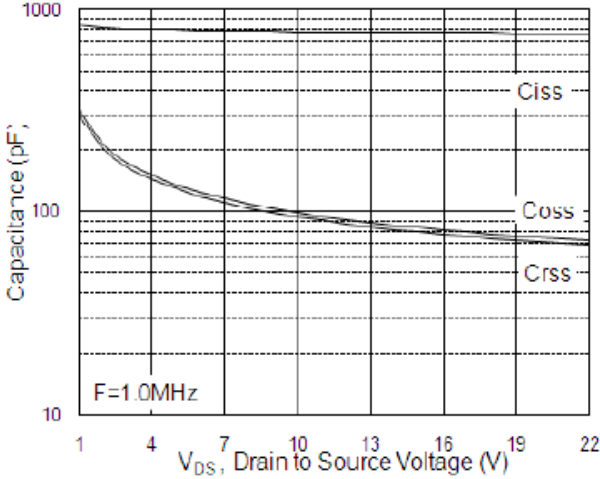


Fig. 7 Capacitance vs Vds

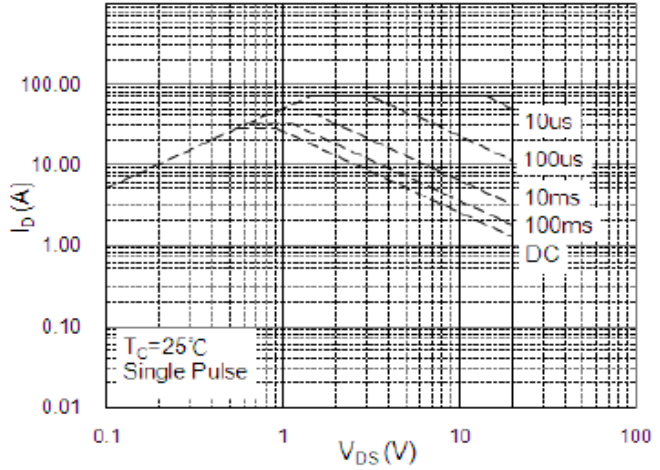


Fig. 8 Safe Operation Region

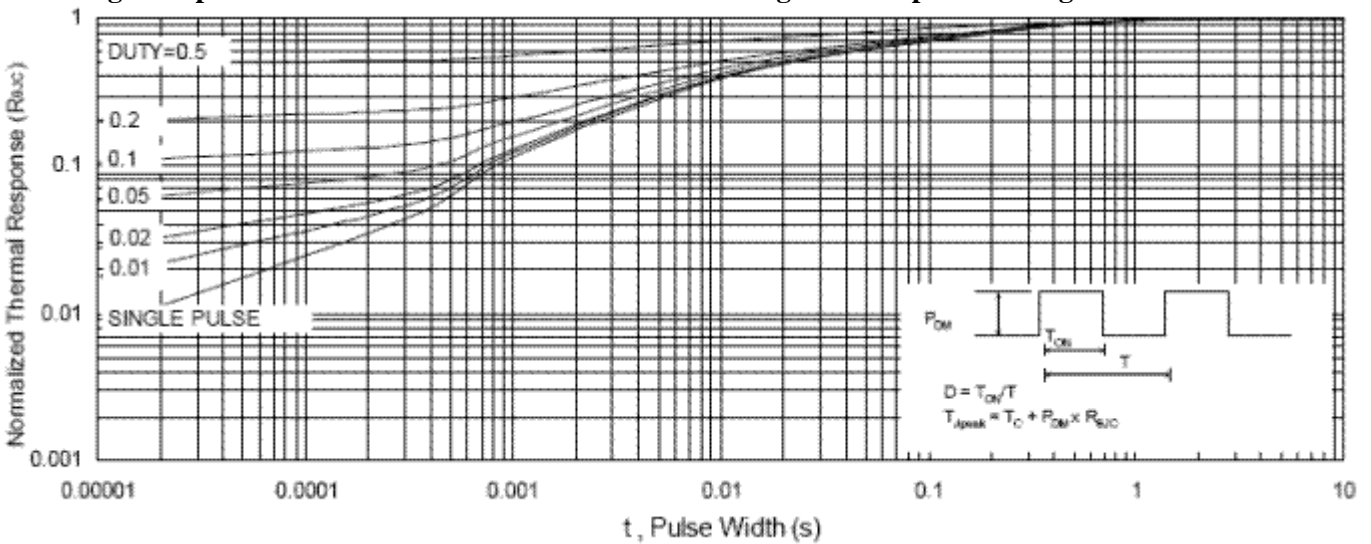


Fig. 9 Maximum Transient Thermal Impedance

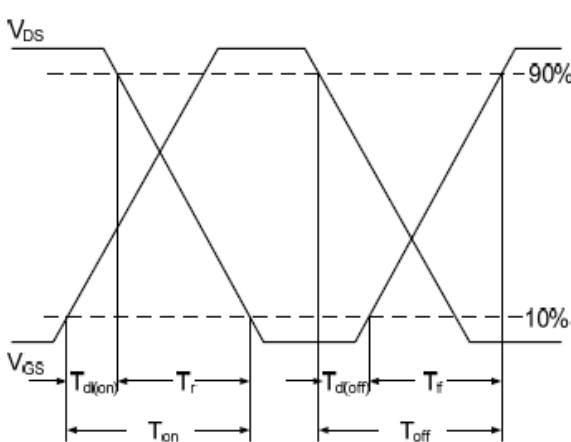


Fig. 10 Switching Time Waveform

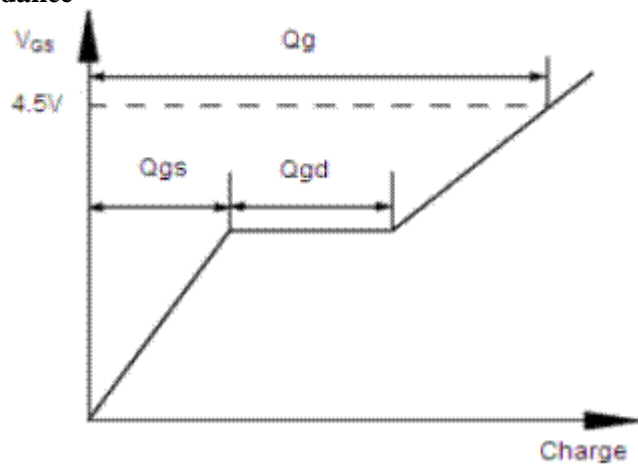
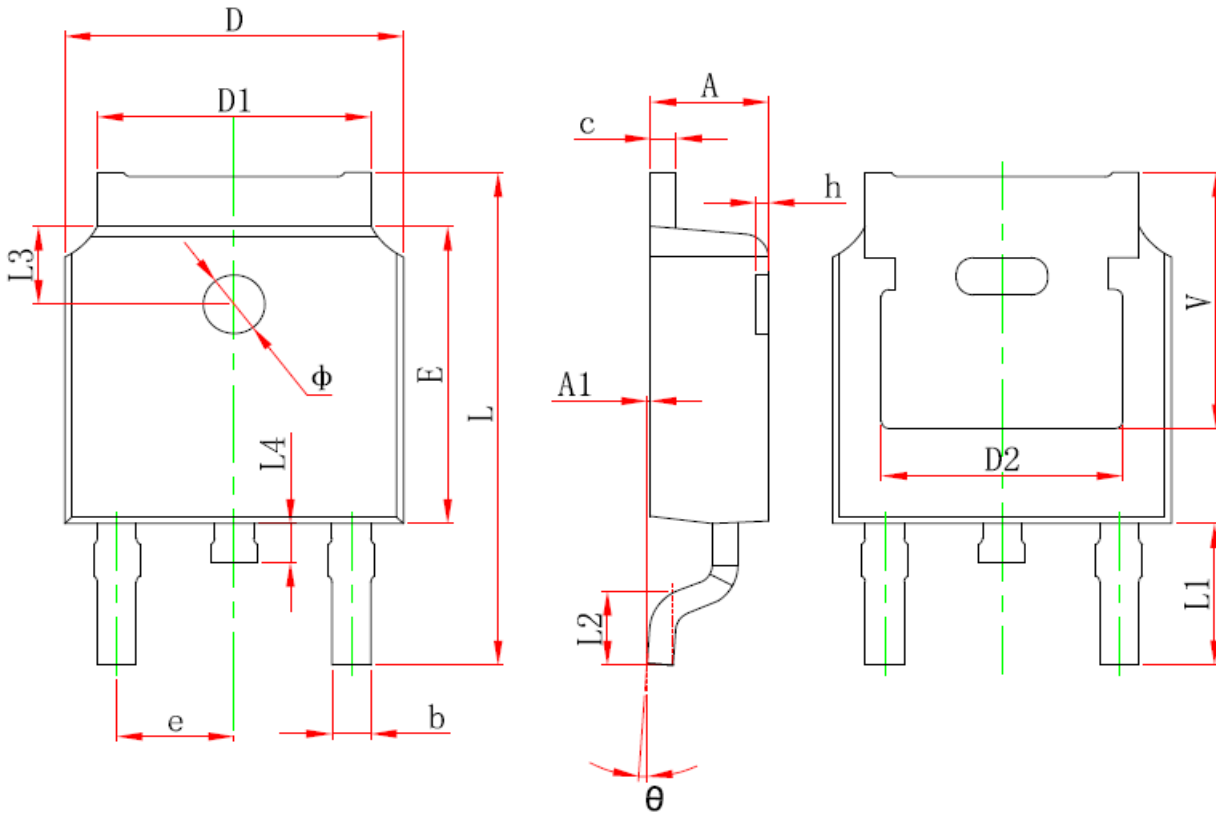


Fig. 11 Gate Charge Waveform



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TO-252 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	



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