SPN220N04
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN220N04 is the N-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN220N04 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

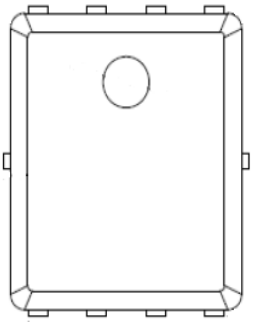
APPLICATIONS

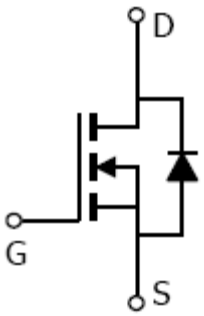
- High Frequency Synchronous Buck Converter
- DC/DC Power System
- Load Switch

FEATURES

- 40V/220A,$R_{DS(ON)}$=1.1mΩ@V_{GS}=10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK5x6-8L package design

PIN CONFIGURATION(PPAK5x6-8L)





PART MARKING

A : Lot Code
B : Date Code
(YY / MM / DD)

SPN220N04
N-Channel Enhancement Mode MOSFET

PPAK5x6-8L PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN220N04DN8RGB	PPAK5x6-8L	SPN220N04

※ SPN220N04DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	40	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	T_C=25℃	I_D	220	A
	T_C=100℃		140	
Pulsed Drain Current		I_{DM}	400	A
Avalanche Current		I_{AS}	116	A
Single Pulse Avalanche Energy		EAS	673	mJ
Power Dissipation	T_C=25℃	P_D	83	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case		$R_{\theta JC}$	1.5	℃/W
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	55	℃/W

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2.0	2.8	4.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=32V,V_{GS}=0V			1	uA
		V_{DS}=32V,V_{GS}=0V,T_J=55℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥5V,V_{GS}=10V			100	A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		0.9	1.1	mΩ
Gate Resistance	Rg	V_{DS}=V_{GS} =0V, f=1MHz		1.2		Ω
Diode Forward Voltage	V_{SD}	I_S=1A,V_{GS}=0V			1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=20V,V_{GS}=10V I_D=20A		108		nC
Gate-Source Charge	Q_{gs}			25.4		
Gate-Drain Charge	Q_{gd}			26.8		
Input Capacitance	C_{iss}	V_{DS}=20V,V_{GS}=0V f=1MHz		6601		pF
Output Capacitance	C_{oss}			2073		
Reverse Transfer Capacitance	C_{rss}			248		
Turn-On Time	$t_{d(on)}$	V_{DD}=20V, I_D=20A,V_{GEN}=10V R_G=1.5Ω		20		nS
	t_r			145		
Turn-Off Time	$t_{d(off)}$			55		
	t_f			18		

TYPICAL CHARACTERISTICS

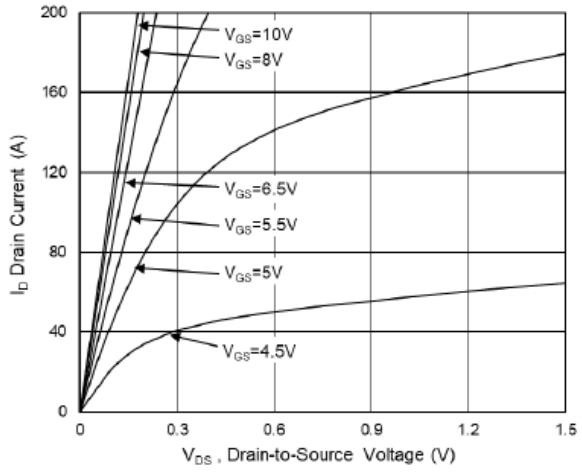


Fig.1 Typical Output Characteristics

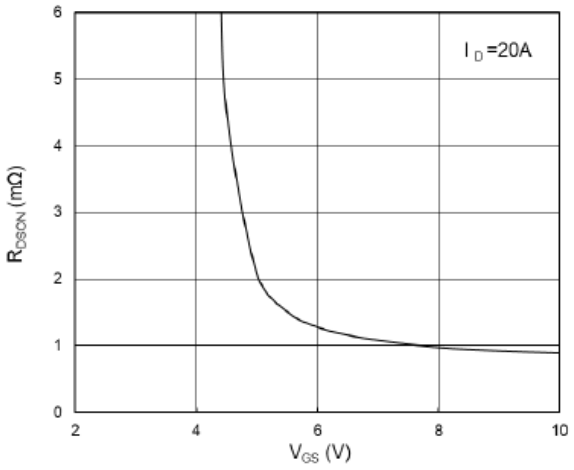


Fig.2 On-Resistance vs G-S Voltage

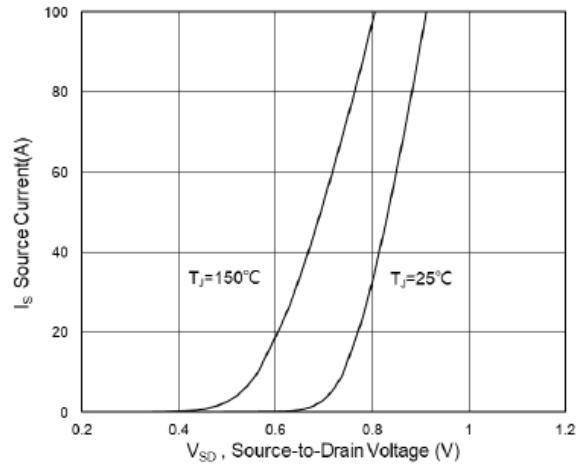


Fig.3 Source Drain Forward Characteristics

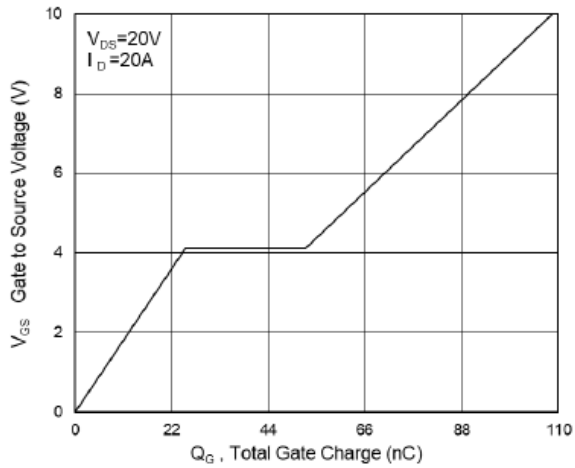


Fig.4 Gate-Charge Characteristics

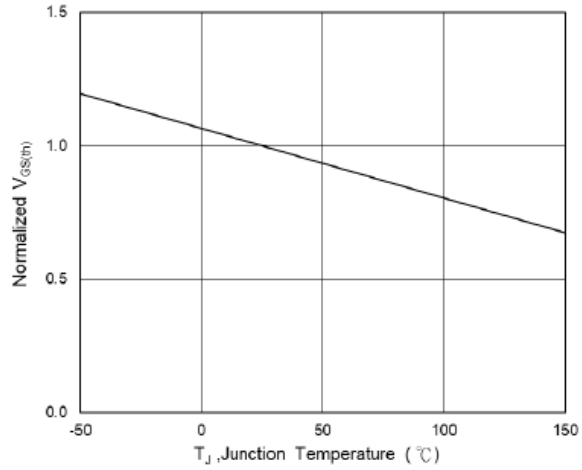


Fig.5 Normalized $V_{GS(th)}$ vs T_J

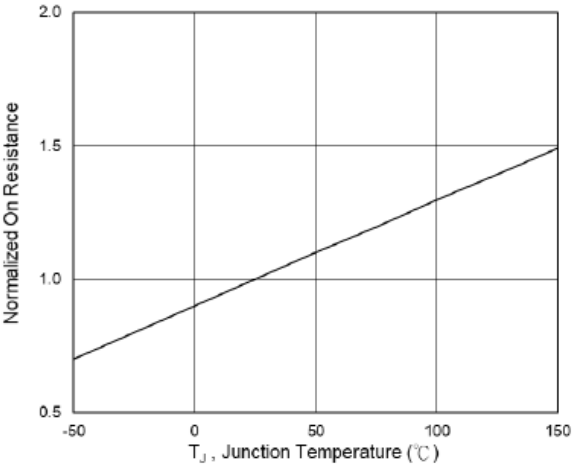


Fig.6 Normalized R_{DSON} vs T_J

TYPICAL CHARACTERISTICS

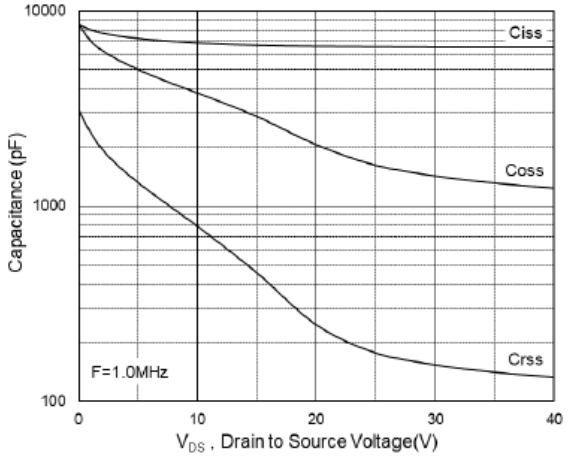


Fig.7 Capacitance

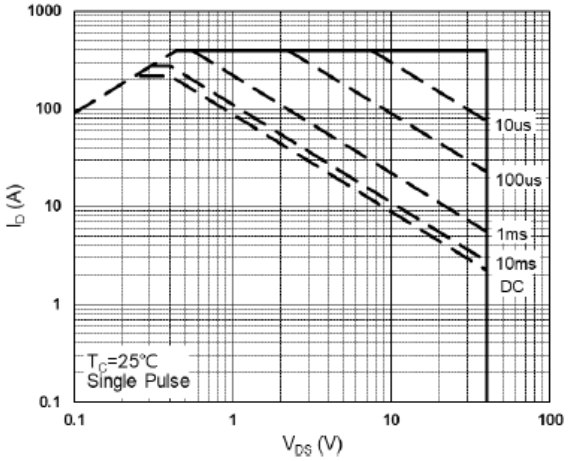


Fig.8 Safe Operating Area

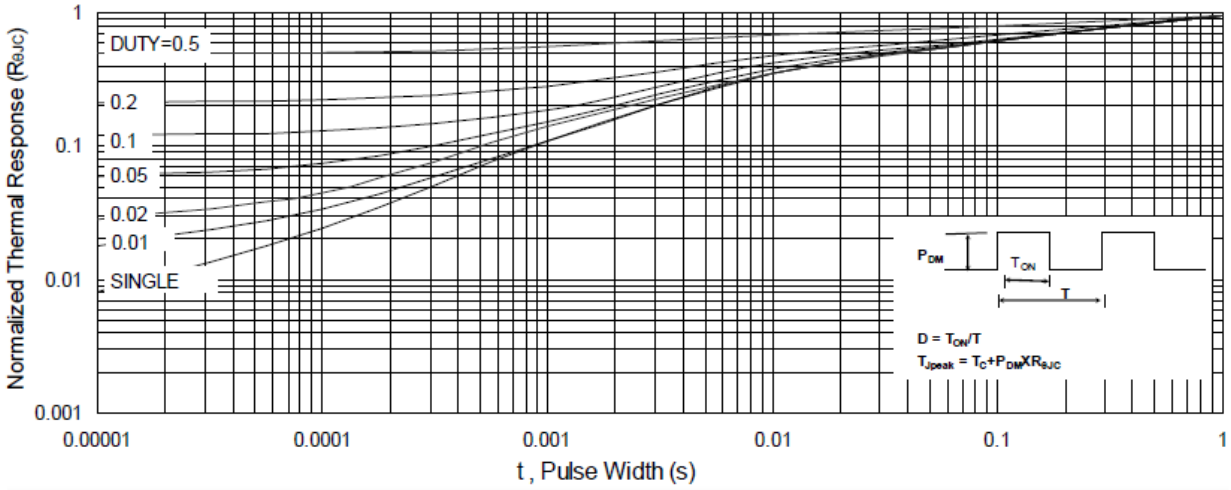


Fig.9 Normalized Maximum Transient Thermal Impedance

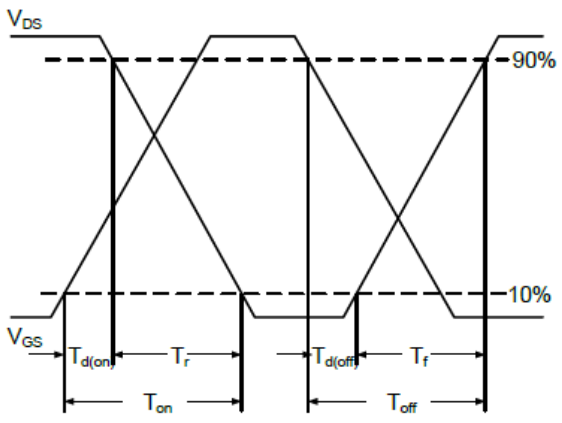


Fig.10 Switching Time Waveform

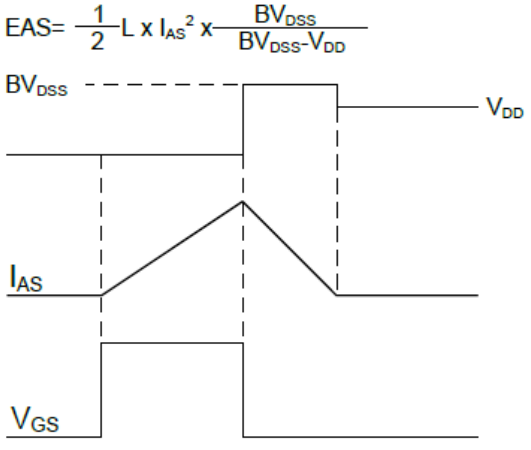


Fig.11 Unclamped Inductive Switching Waveform

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