



# SPN2318

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN2318 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

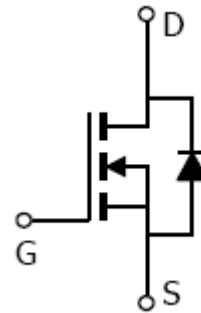
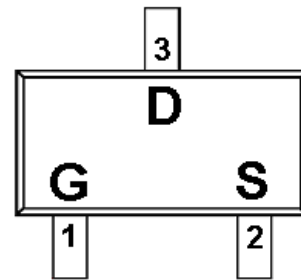
### FEATURES

- ◆ 40V/3.9A, $R_{DS(ON)}= 56m\Omega@V_{GS}=10V$
- ◆ 40V/3.5A, $R_{DS(ON)}= 62m\Omega@V_{GS}=4.5V$
- ◆ 40V/2.0A, $R_{DS(ON)}= 95 m\Omega@V_{GS}= 2.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23-3L package design

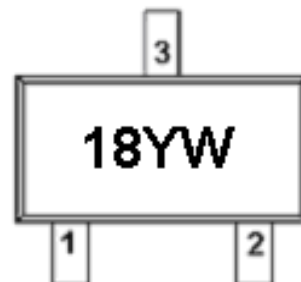
### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

### PIN CONFIGURATION ( SOT-23-3L )



### PART MARKING



Y : Year Code  
W : Week Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN2318S23RGB	SOT-23-3L	18YW

※ Week Code : A ~ Z( 1 ~ 26 ) ; a ~ z( 27 ~ 52 )

※ SPN2318S23RGB : Tape Reel ; Pb – Free ; Halogen -Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	40	V
Gate –Source Voltage	V <sub>GSS</sub>	±12	V
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	4.0
		TA=70°C	3.0
Pulsed Drain Current	I <sub>DM</sub>	10	A
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	1.25	A
Power Dissipation	P <sub>D</sub>	TA=25°C	1.25
		TA=70°C	0.8
Operating Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	100	°C/W



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### ELECTRICAL CHARACTERISTICS

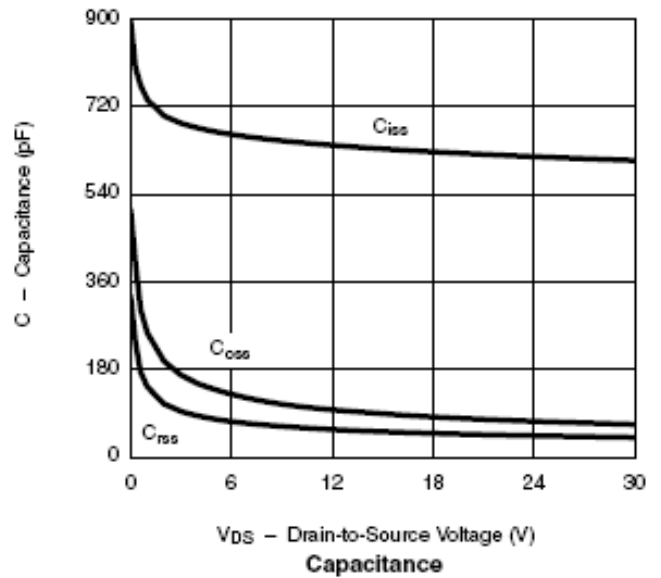
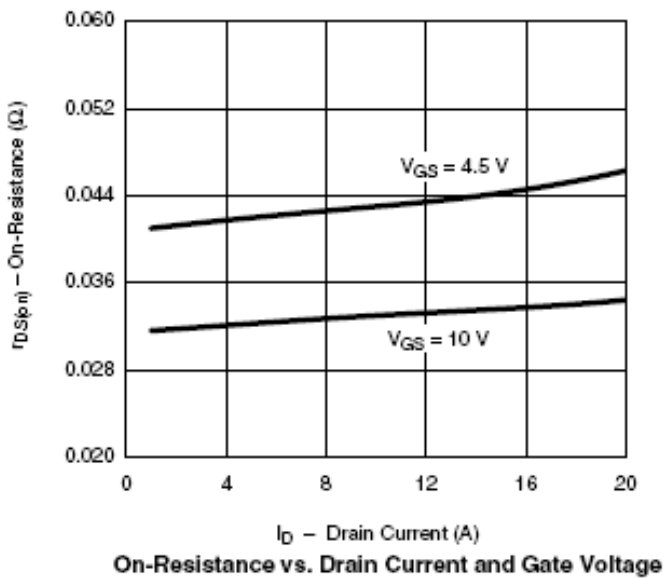
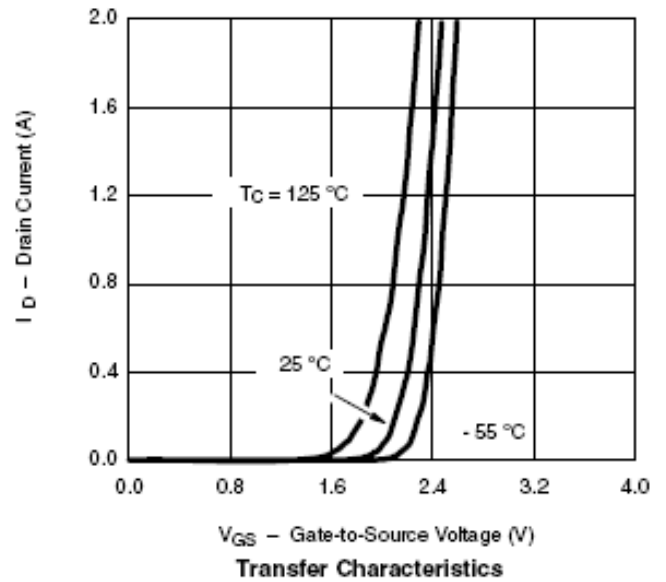
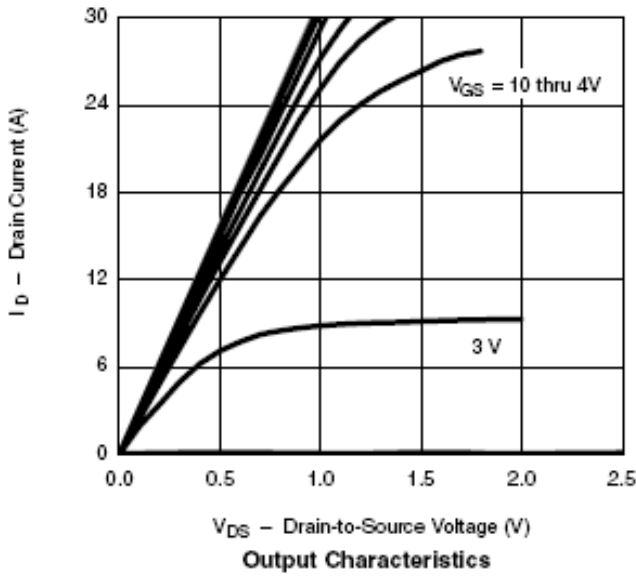
( $T_A=25^{\circ}\text{C}$  Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5		1.2	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$			1	uA
		$V_{DS}=40V, V_{GS}=0V$ $T_J=85^{\circ}\text{C}$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}= 5V, V_{GS}=4.5V$	10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}= 10V, I_D=3.9A$		0.050	0.056	$\Omega$
		$V_{GS}=4.5V, I_D=3.5A$		0.056	0.062	
		$V_{GS}=2.5V, I_D=2.0A$		0.088	0.095	
Forward Transconductance	$g_{fs}$	$V_{DS}=15V, I_D=6.2A$		13		S
Diode Forward Voltage	$V_{SD}$	$I_S=2.3A, V_{GS}=0V$		0.8	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=15V, V_{GS}=10V$ $I_D= 2A$		10	15	nC
Gate-Source Charge	$Q_{gs}$			1.6		
Gate-Drain Charge	$Q_{gd}$			2.0		
Input Capacitance	$C_{iss}$	$V_{DS}=20V, V_{GS}=0V$ $f=1\text{MHz}$		500		pF
Output Capacitance	$C_{oss}$			80		
Reverse Transfer Capacitance	$C_{rss}$			45		
Turn-On Time	$t_{d(on)}$	$V_{DD}=15V, R_L=15\Omega$ $I_D=1.0A, V_{GEN}=10V$ $R_G=6\Omega$		15	20	nS
	$t_r$			6	12	
Turn-Off Time	$t_{d(off)}$			10	20	
	$t_f$			40	80	



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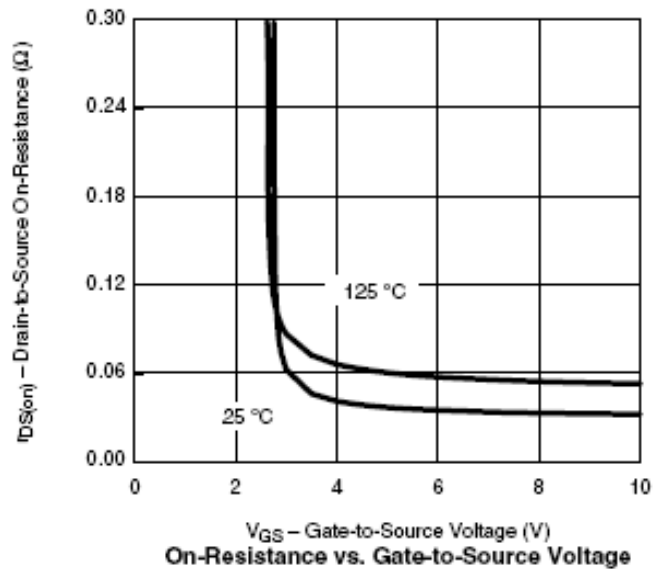
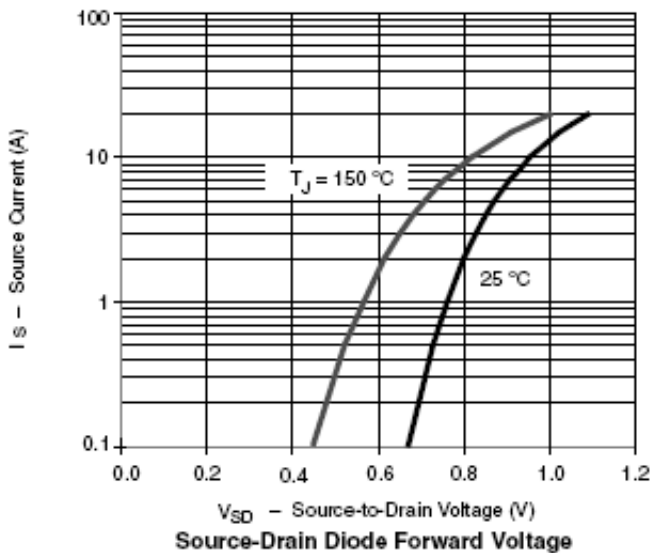
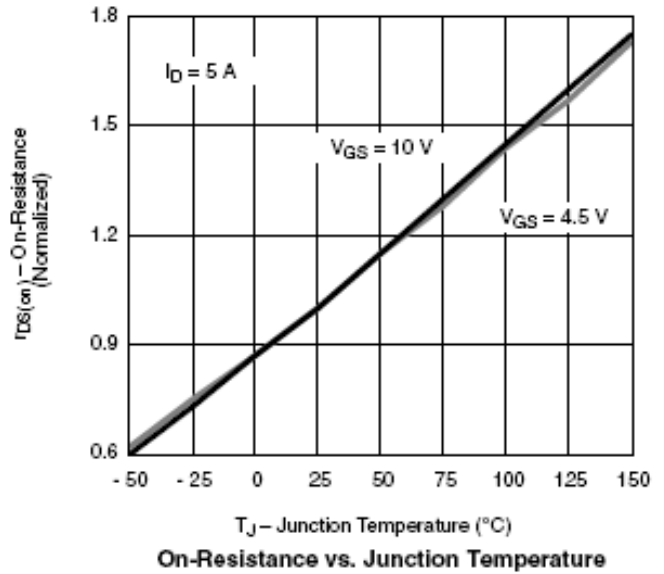
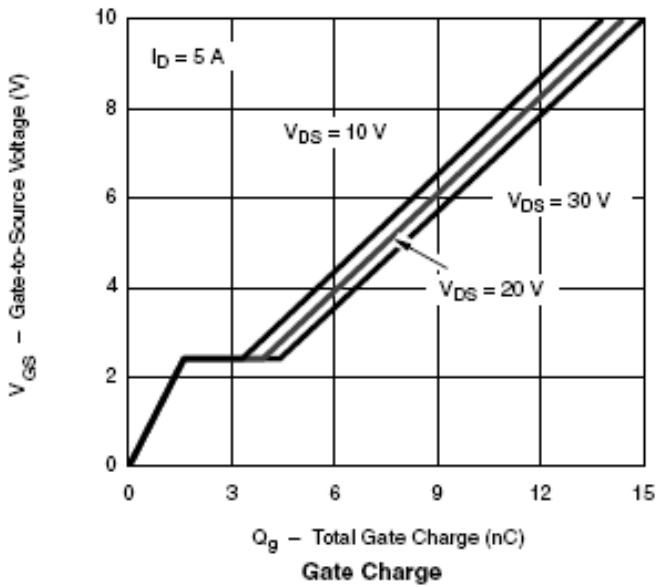
## TYPICAL CHARACTERISTICS





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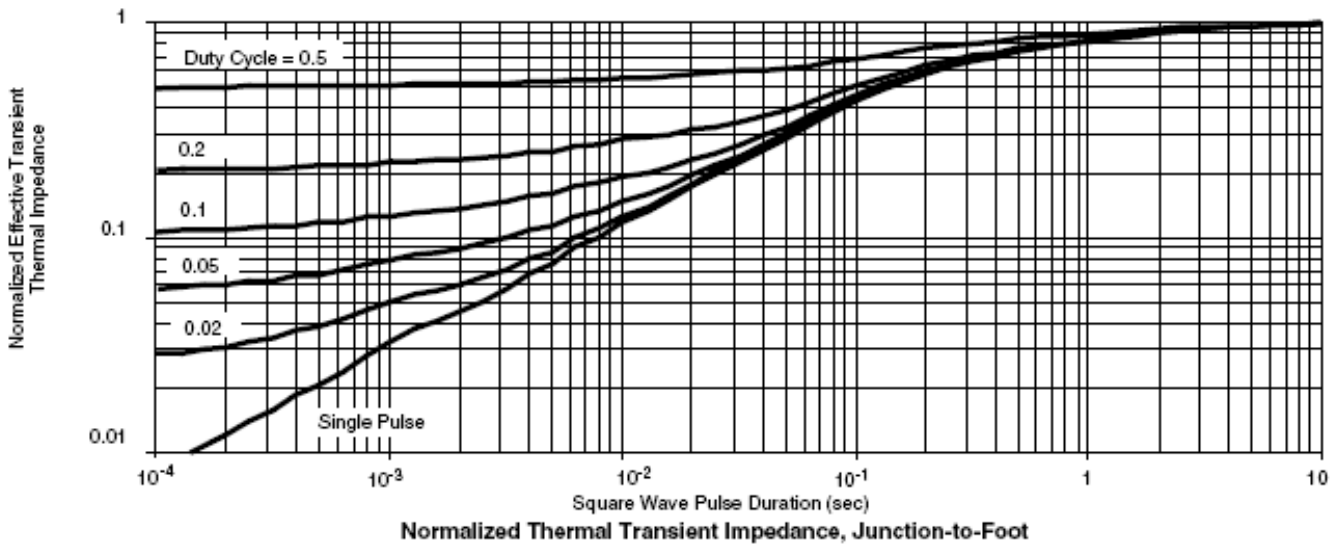
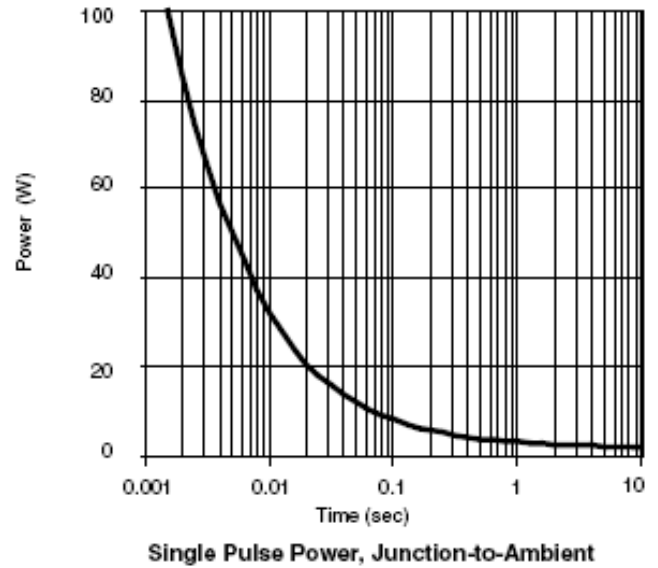
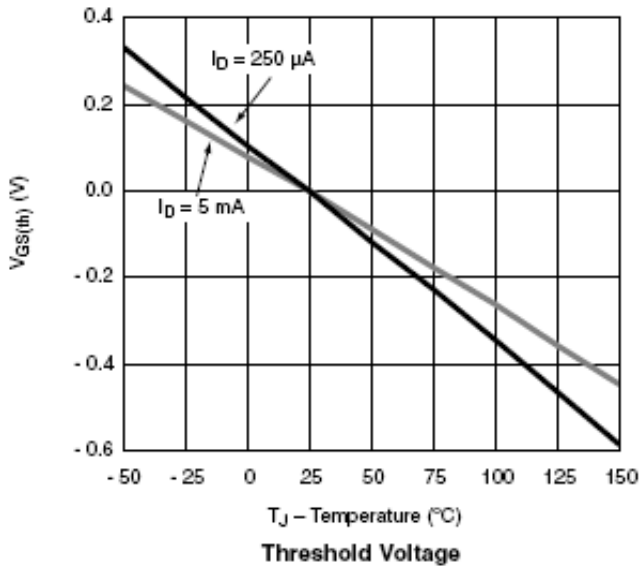
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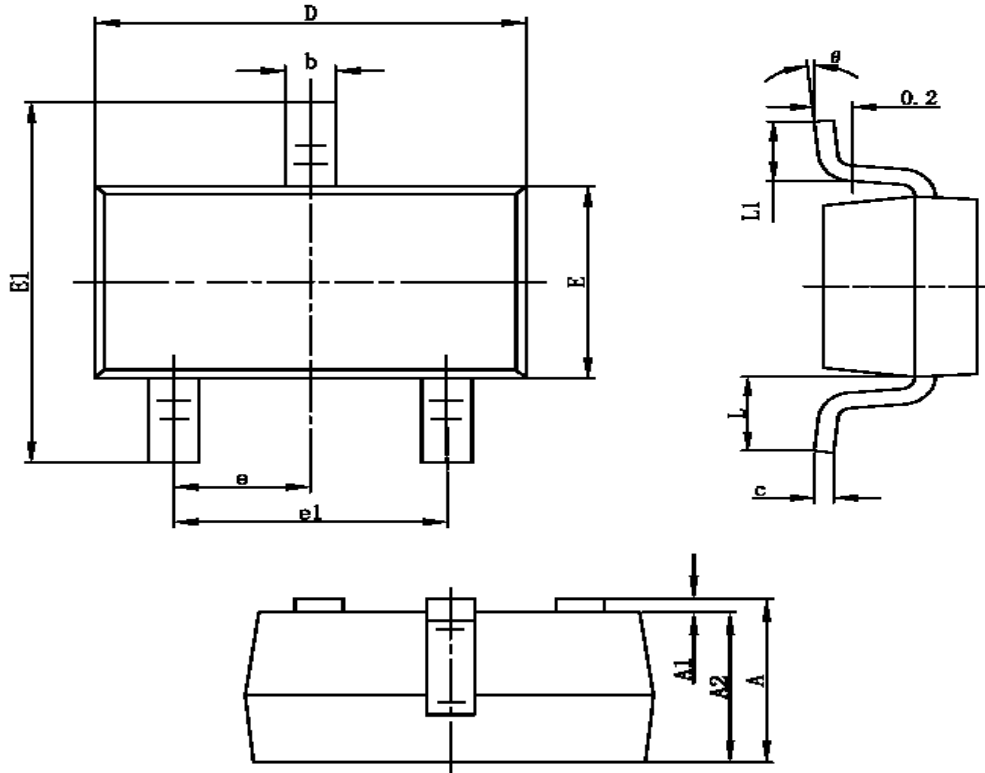




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### SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



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