



# SPN340T06

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN340T06 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low RDS(ON) and fast switching speed..

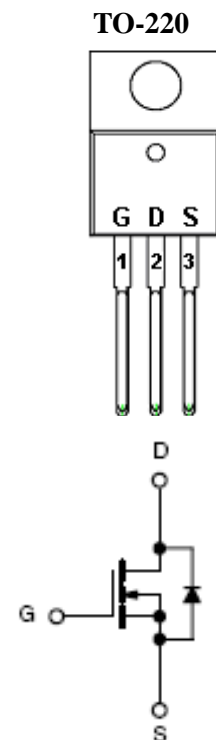
### FEATURES

- ◆ 60V/340A, RDS(ON)=1.9mΩ@VGS=10V
- ◆ Super high density cell design for extremely low RDS (ON)
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ Enhanced Avalanche Ruggedness
- ◆ TO-220-3L package design

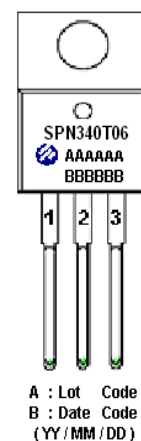
### APPLICATIONS

- DC/DC Converter
- Hard Switching and High Speed Circuit
- Synchronous Buck Converter
- Power Tools
- UPS
- Motor Control

### PIN CONFIGURATION



### PART MARKING





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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN340T06T220TGB	TO-220-3L	SPN340T06

※ SPN340T06T220TGB: Tube ; Pb – Free; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS

( $T_A=25^{\circ}\text{C}$  Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	$V_{DS}$	60	V	
Gate –Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current(Silicon Limited)	$I_D$	$T_C=25^{\circ}\text{C}$	340	A
		$T_C=70^{\circ}\text{C}$	240	
Continuous Drain Current(Package Limited)	$T_C=25^{\circ}\text{C}$	120		
Pulsed Drain Current	$I_{DM}$	900	A	
Power Dissipation	$P_D$	104	W	
Avalanche Energy with Single Pulse ( $T_C=25^{\circ}\text{C}$ , $L = 0.4\text{mH}$ )	EAS	1280	mJ	
Operating Junction Temperature	$T_J$	-55/150	$^{\circ}\text{C}$	
Storage Temperature Range	$T_{STG}$	-55/150	$^{\circ}\text{C}$	
Thermal Resistance-Junction to Case	$R_{\theta JC}$	1.2	$^{\circ}\text{C}/\text{W}$	



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$ $T_J = 25^\circ C$			1	uA
		$V_{DS}=60V, V_{GS}=0V$ $T_J = 100^\circ C$			100	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS} = 10V$	60			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		1.67	1.9	mΩ
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=20A$		92		S
Gate Resistance	$R_G$	$V_{GS}=0V, V_{DS}=\text{Open},$ $f=1MHz$		0.7		Ω
Diode Forward Voltage	$V_{SD}$	$I_F=20A, V_{GS} = 0V$		0.9	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=30V, V_{GS}=10V$ $I_D=20A$		124		nC
Gate-Source Charge	$Q_{gs}$			30		
Gate-Drain Charge	$Q_{gd}$			20		
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V$ $f=1MHz$		10570		pF
Output Capacitance	$C_{oss}$			4050		
Reverse Transfer Capacitance	$C_{rss}$			84		
Turn-On Time	$t_{d(on)}$	$V_{DD}=30V, I_D=20A,$ $V_{GS}=10V, R_G=3\Omega$		35		nS
	$t_r$			27		
Turn-Off Time	$t_{d(off)}$			70		
	$t_f$			15		



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### TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

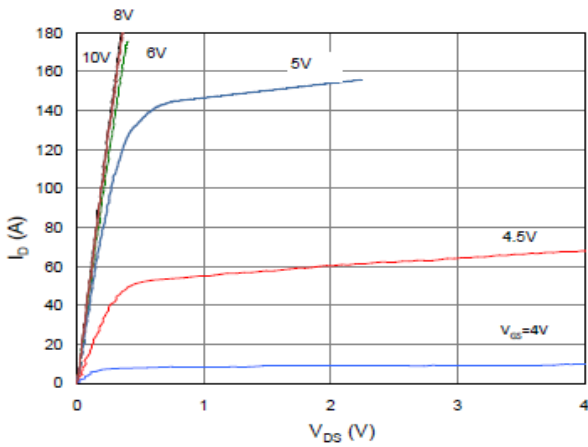


Figure 2. On-Resistance vs. Gate-Source Voltage

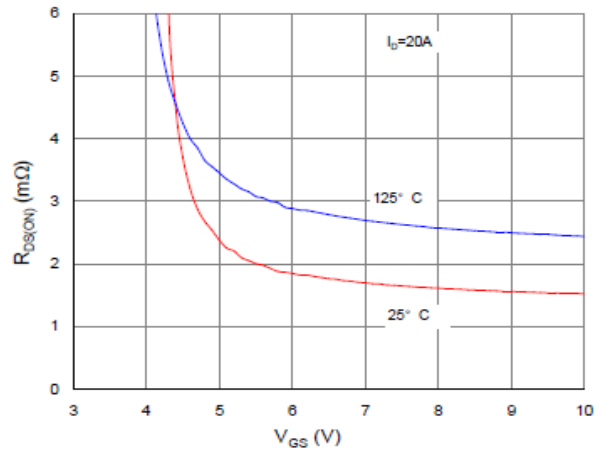


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

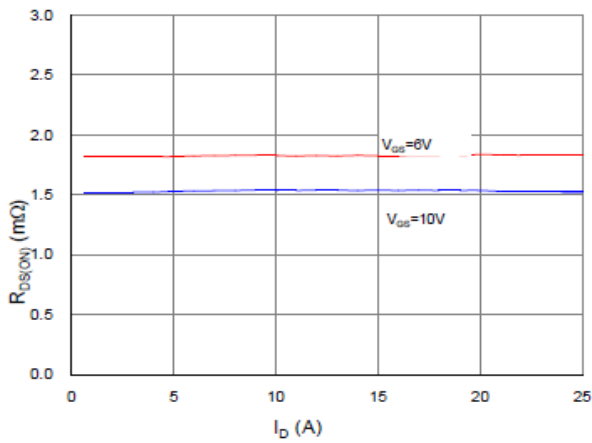


Figure 4. Normalized On-Resistance vs. Junction Temperature

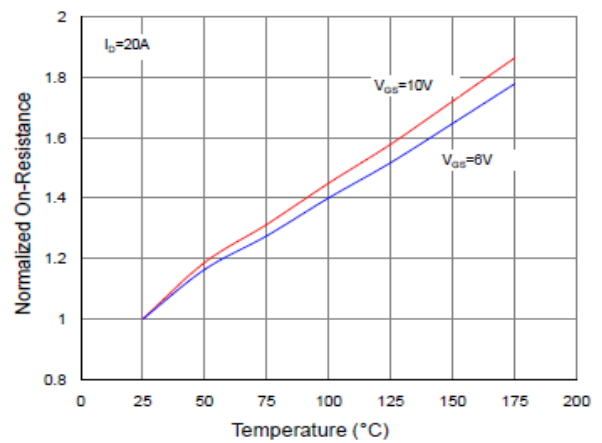


Figure 5. Typical Transfer Characteristics

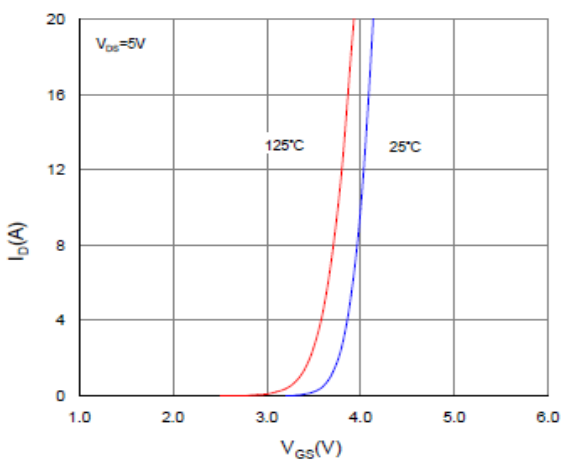
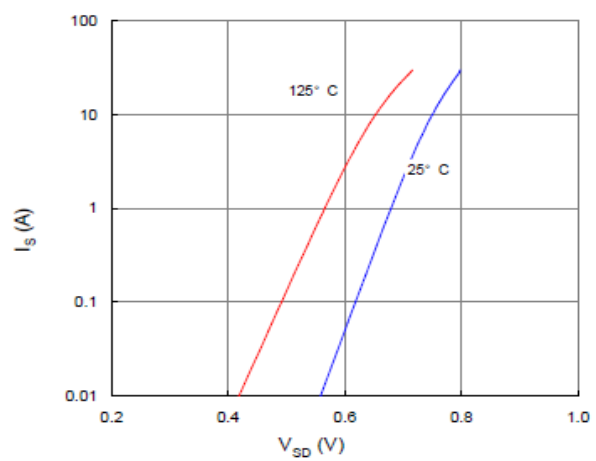


Figure 6. Typical Source-Drain Diode Forward Voltage





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### TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

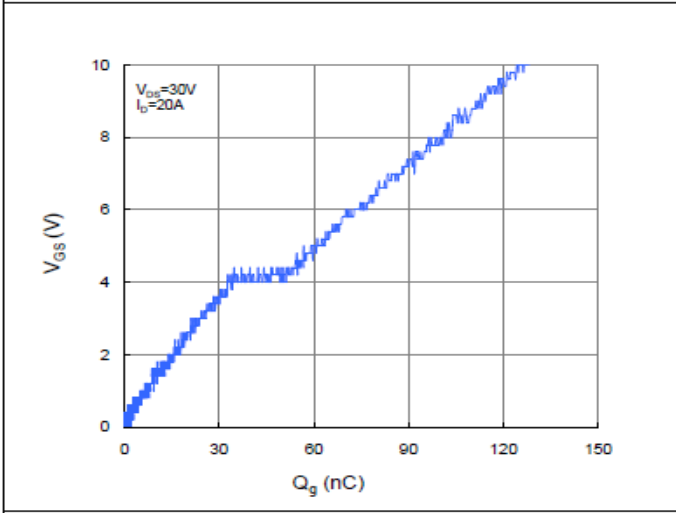


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

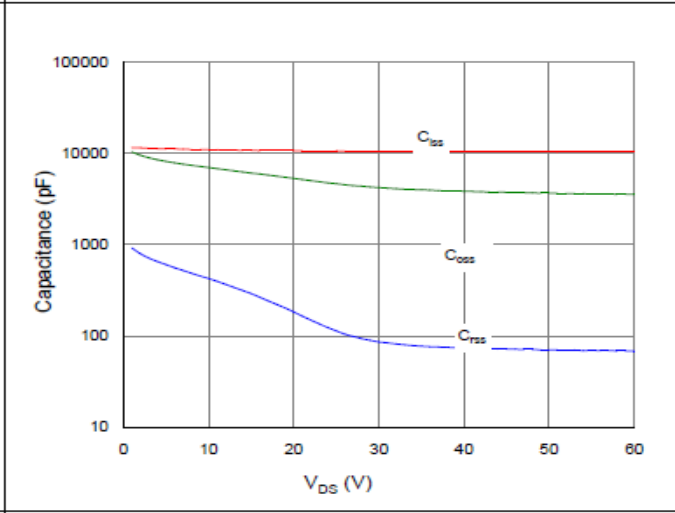


Figure 9. Maximum Safe Operating Area

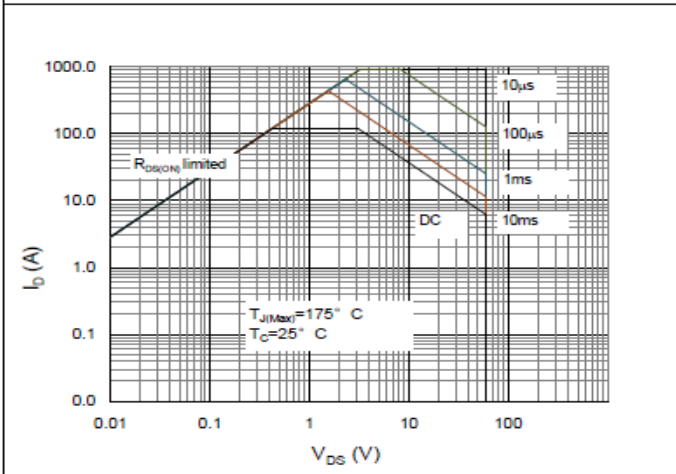


Figure 10. Maximum Drain Current vs. Case Temperature

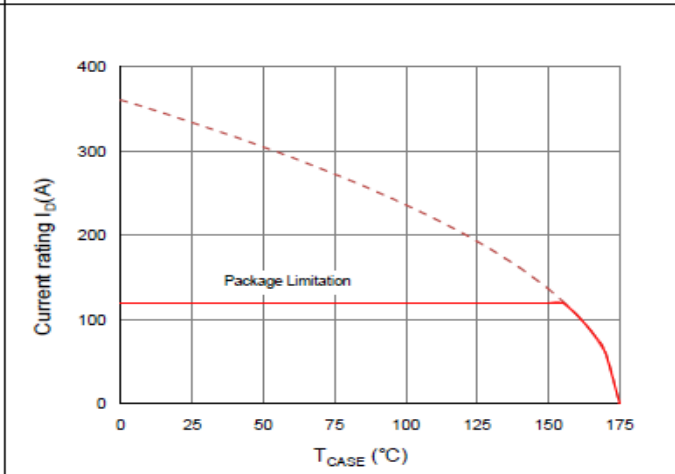
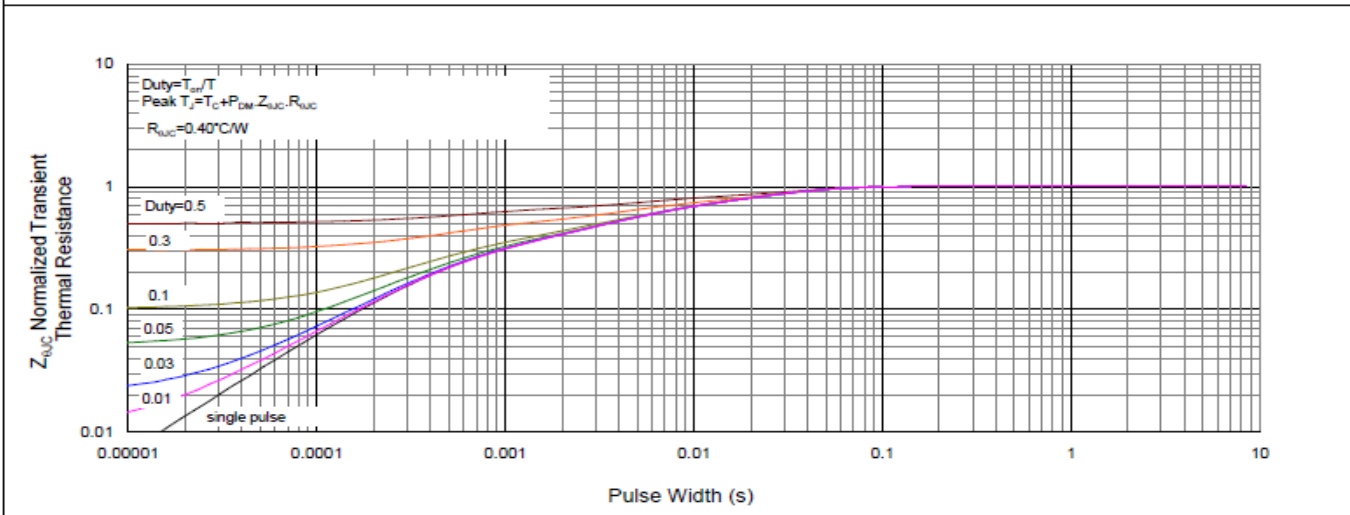


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

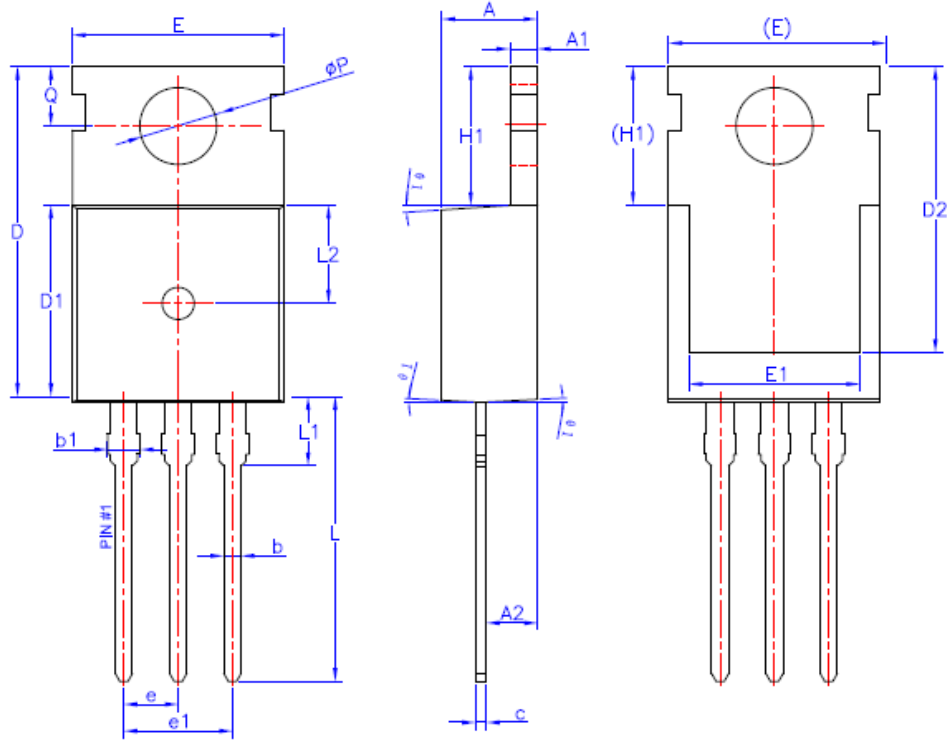




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### TO-220-3L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	0.60	0.90
b1	-	-	1.40
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	-	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	-	-	3.50
L2	4.6REF		
$\phi P$	3.55	3.60	3.65
Q	2.73	-	2.87
$\theta 1$	1°	3°	5°



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