



SPN3422

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN3422 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

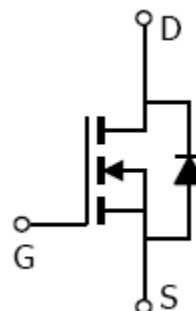
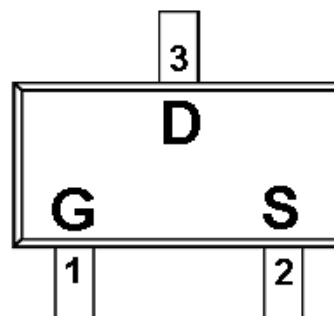
FEATURES

- ◆ 60V/3.0A, $R_{DS(ON)}=125m\Omega@V_{GS}=10V$
- ◆ 60V/2.5A, $R_{DS(ON)}=145m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

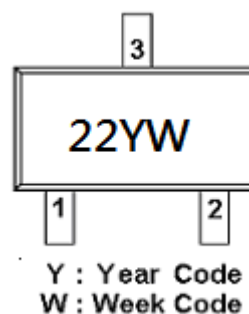
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION (SOT-23)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN3422S23RGB	SOT-23	22

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPN3422S23RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	60	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	3.0	A
		2.2	
Pulsed Drain Current	I _{DM}	6	A
Continuous Source Current(Diode Conduction)	I _S	2.0	A
Power Dissipation	P _D	2.0	W
		1.3	
Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	140	°C/W



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ELECTRICAL CHARACTERISTICS

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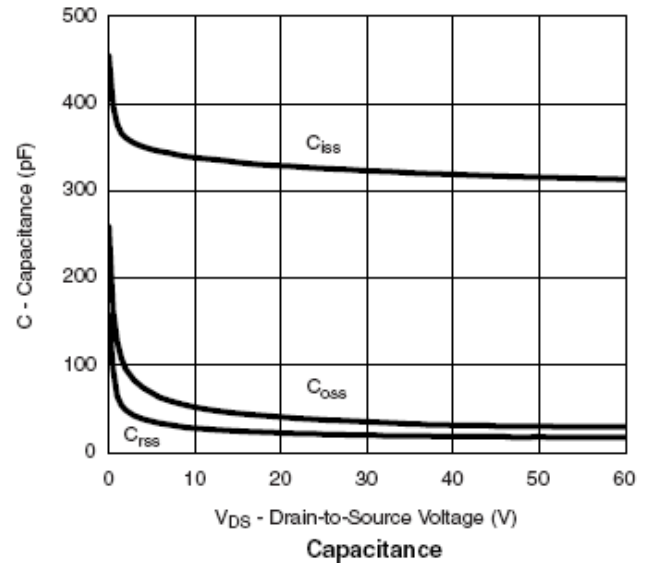
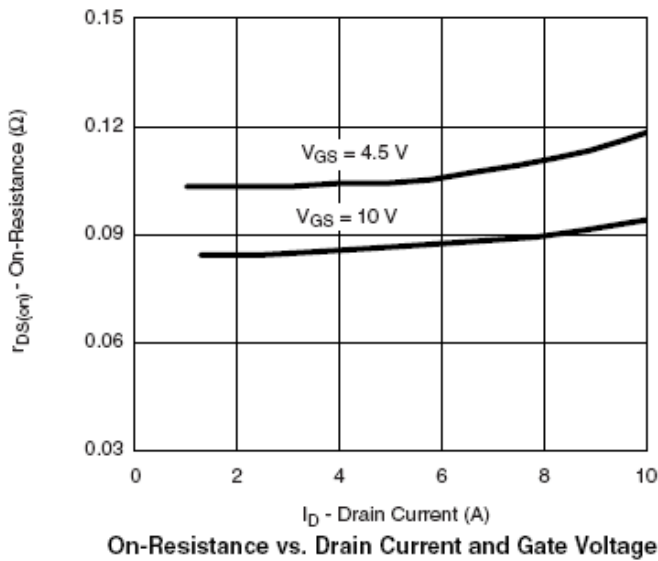
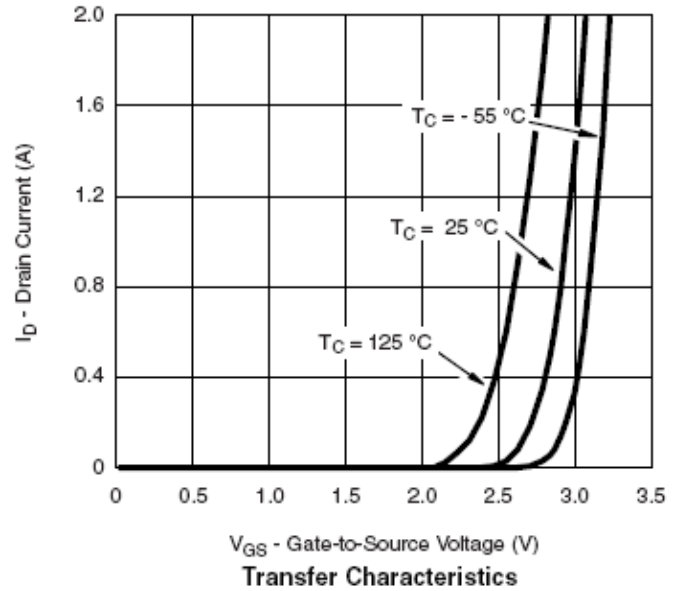
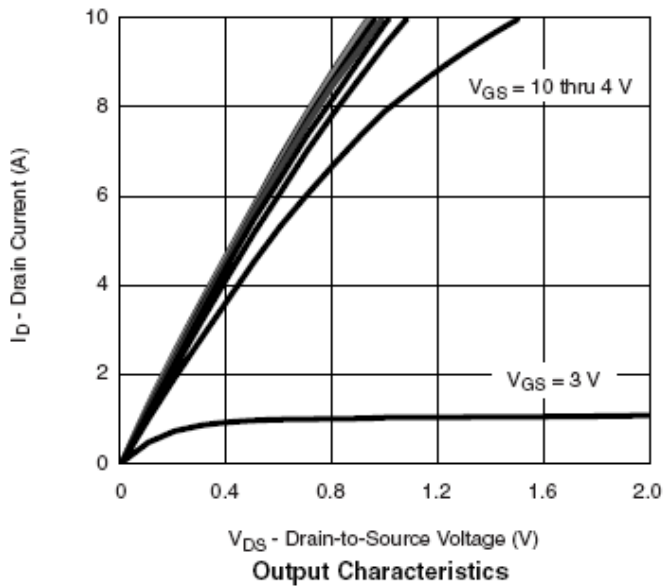
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.5		1.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =48V, V _{GS} =0.0V			1	μA
		V _{DS} =48V, V _{GS} =0.0V T _J =55°C			10	
On-State Drain Current	I _{D(on)}	V _{DS} ≥ 4.5V, V _{GS} =4.5V	10			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =3.0A		0.106	0.125	Ω
		V _{GS} = 4.5V, I _D =2.5A		0.118	0.145	
Forward Transconductance	g _{fs}	V _{DS} =15V, I _D =4.0A		12		S
Diode Forward Voltage	V _{SD}	I _S =2.5A, V _{GS} =0V		0.8	1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =30V, V _{GS} =4.5V I _D =4.0A		4.0	6	nC
Gate-Source Charge	Q _{gs}			1.2		
Gate-Drain Charge	Q _{gd}			1.0		
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V f=1MHz		320		pF
Output Capacitance	C _{oss}			42		
Reverse Transfer Capacitance	C _{rss}			20		
Turn-On Time	t _{d(on)}	V _{DD} =30V, R _L =12Ω I _D =2.5A, V _{GEN} =10V R _G =6Ω		6	10	nS
	t _r			12	20	
Turn-Off Time	t _{d(off)}			18	30	
	t _f			10	15	



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TYPICAL CHARACTERISTICS

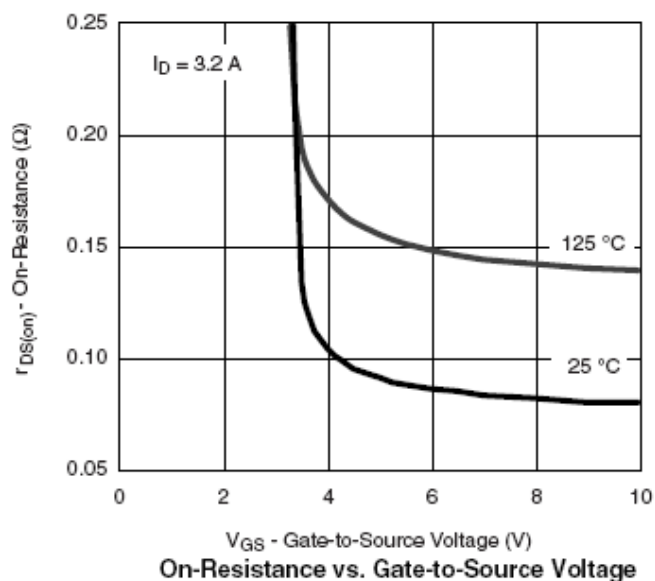
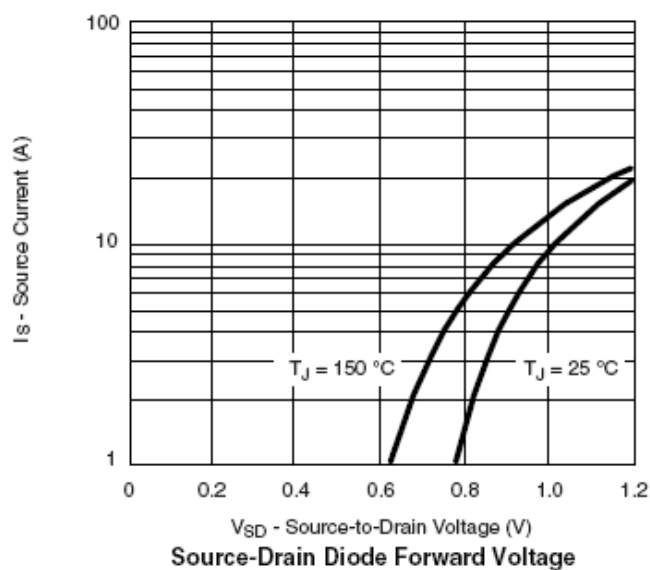
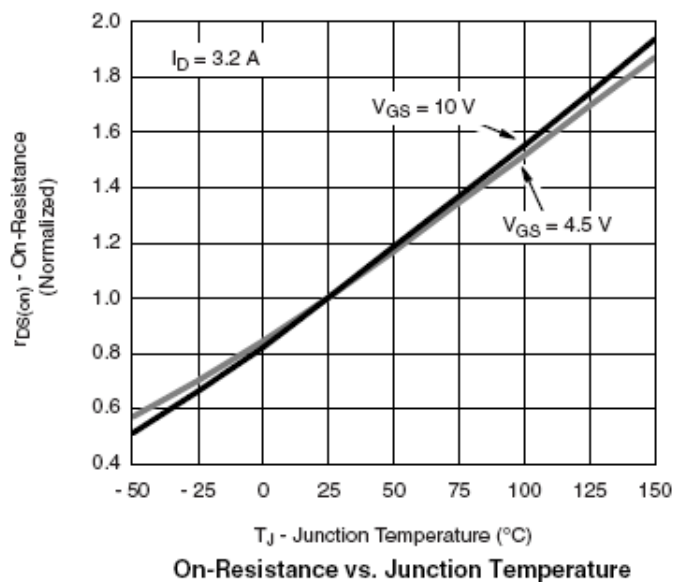
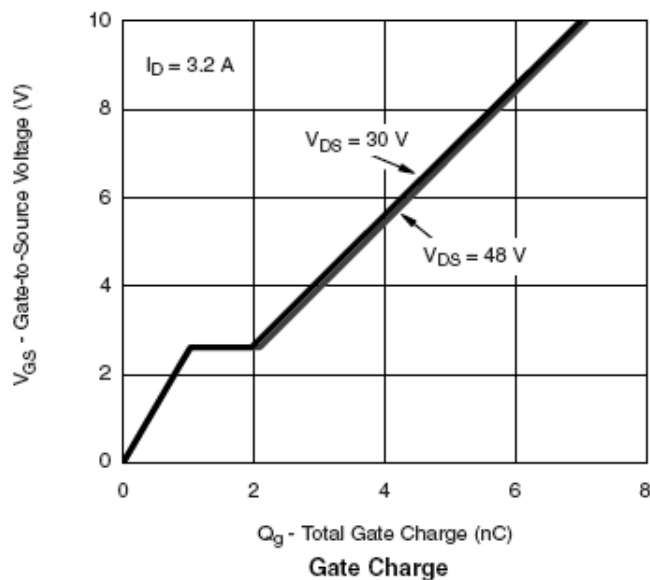




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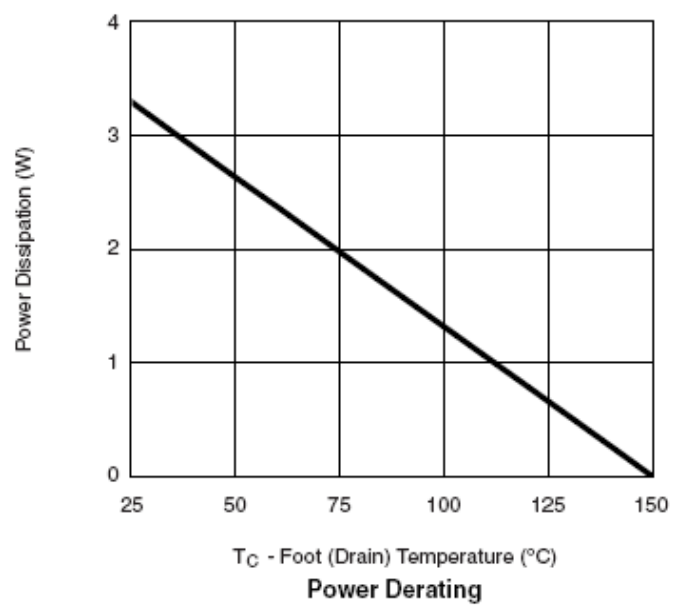
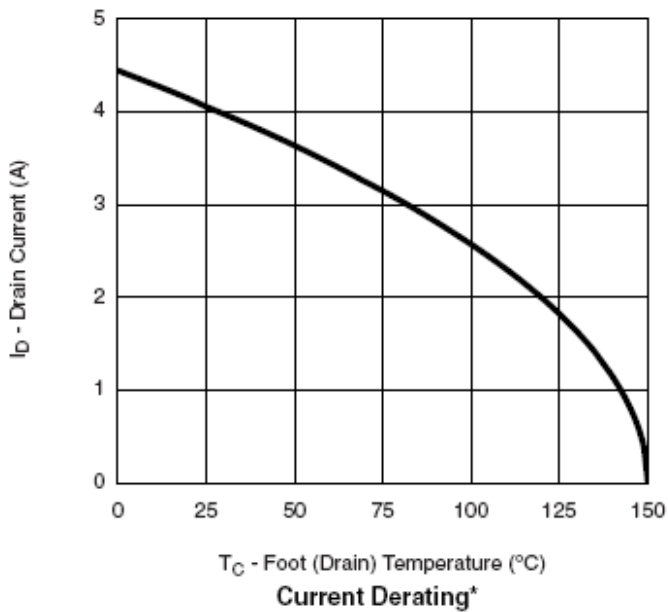
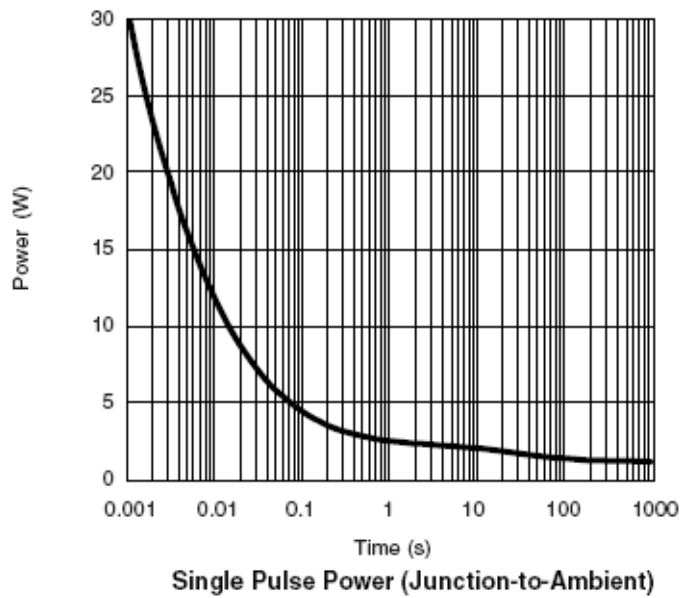
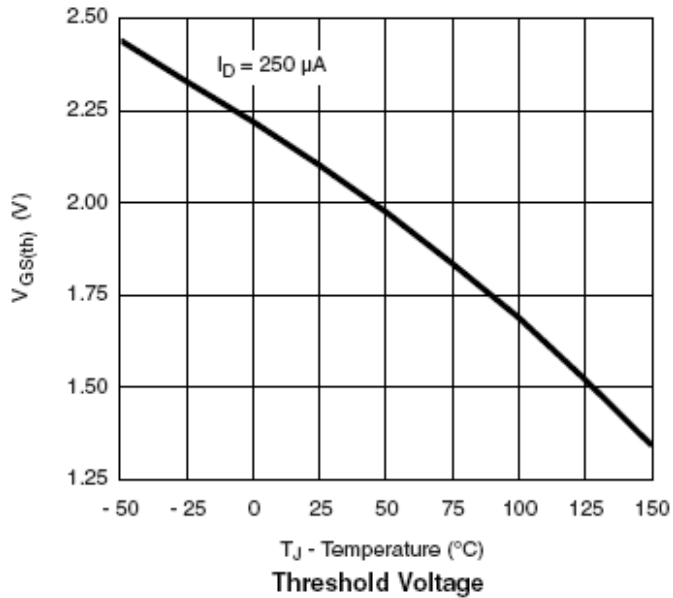




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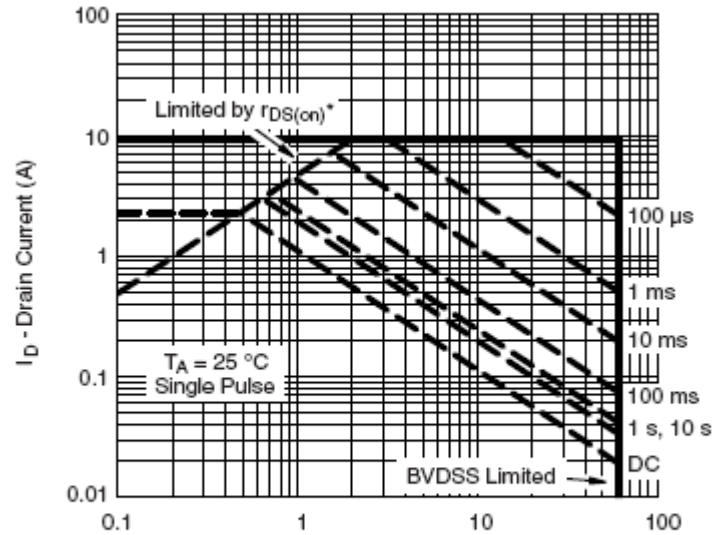




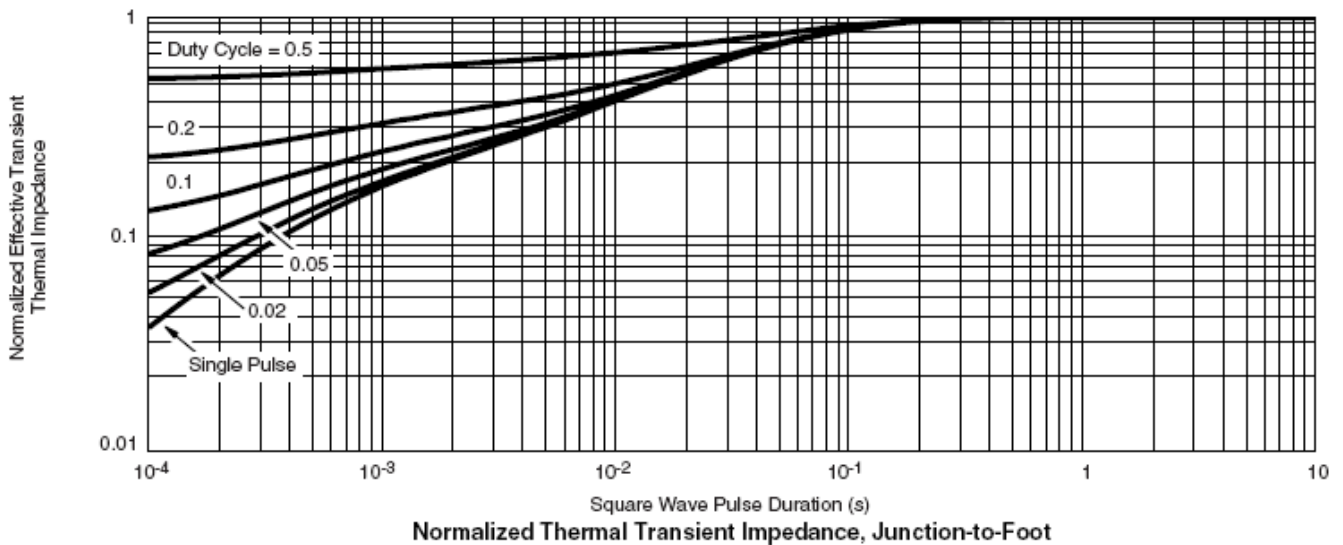
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TYPICAL CHARACTERISTICS



V_{DS} - Drain-to-Source Voltage (V)
* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient





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