



SPN3426

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN3426 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

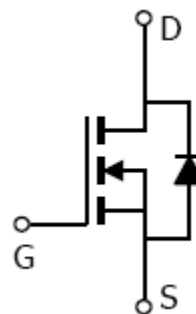
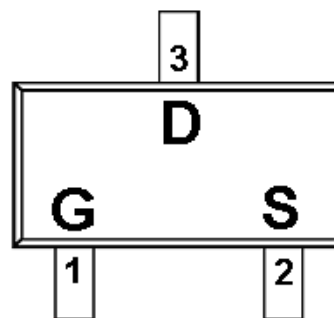
FEATURES

- ◆ 60V/3.0A, $R_{DS(ON)}=90m\Omega@V_{GS}=10V$
- ◆ 60V/2.0A, $R_{DS(ON)}=110m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

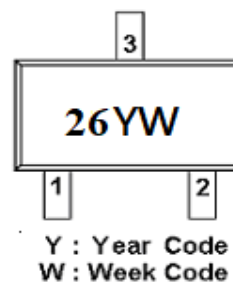
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION (SOT-23)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN3426S23RGB	SOT-23	26

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPN3426S23RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	60	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	T _A =25°C	I _D	3.0	A
	T _A =70°C		2.1	
Pulsed Drain Current		I _{DM}	16	A
Continuous Source Current(Diode Conduction)		I _S	1.5	A
Power Dissipation	T _A =25°C	P _D	1.6	W
	T _A =70°C		1.0	
Operating Junction Temperature		T _J	150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	75	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =48V, V _{GS} =0.0V			1	μA
		V _{DS} =48V, V _{GS} =0.0V T _J =55°C			5	
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =3.0A		80	90	mΩ
		V _{GS} =4.5V, I _D =2.0A		100	110	
Forward Transconductance	g _{fs}	V _{DS} =4.5V, I _D =3.0A		10		S
Diode Forward Voltage	V _{SD}	I _S =1.2A, V _{GS} =0V			1.1	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V, V _{GS} =10V I _D =6.7A		7		nC
Gate-Source Charge	Q _{gs}			1.2		
Gate-Drain Charge	Q _{gd}			3.0		
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V f=1MHz		410		pF
Output Capacitance	C _{oss}			50		
Reverse Transfer Capacitance	C _{rss}			26		
Turn-On Time	t _{d(on)}	V _{DD} =15V, R _L =15Ω I _D =1.0A, V _{GEN} =10V R _G =6Ω		6.0	11	nS
	t _r			8.0	18	
Turn-Off Time	t _{d(off)}			16	29	
	t _f			9	18	



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TYPICAL CHARACTERISTICS

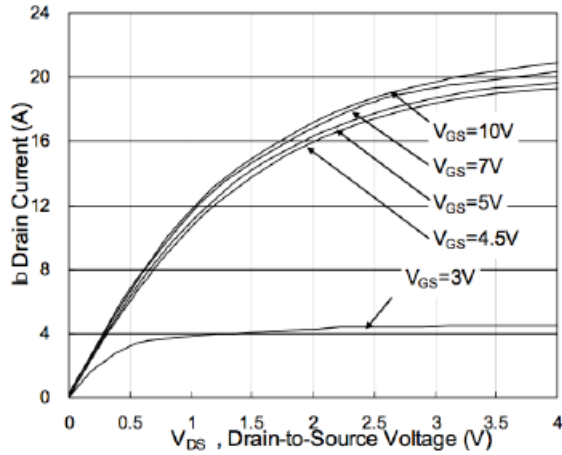


Fig.1 Typical Output Characteristics

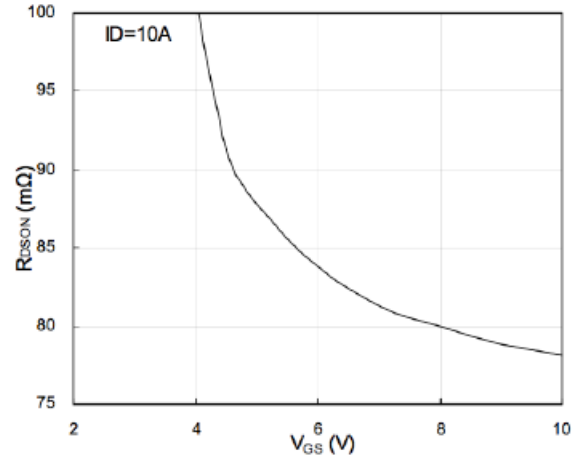


Fig.2 On-Resistance v.s Gate-Source

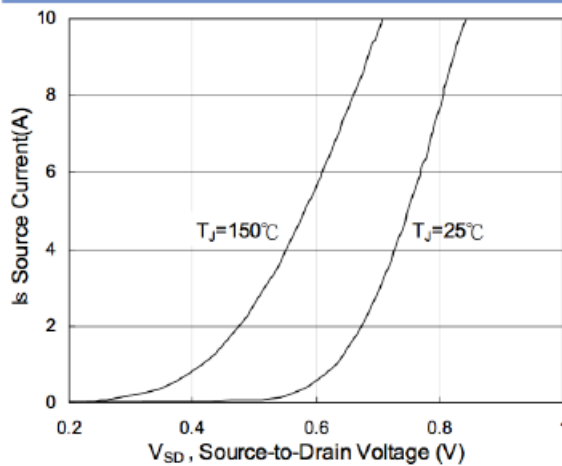


Fig.3 Forward Characteristics of Reverse

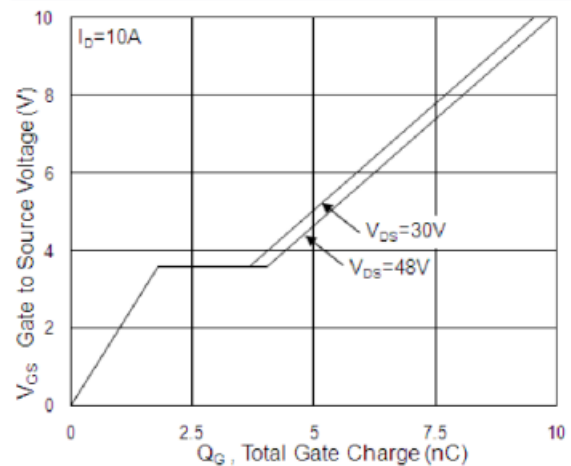


Fig.4 Gate-Charge Characteristics



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TYPICAL CHARACTERISTICS

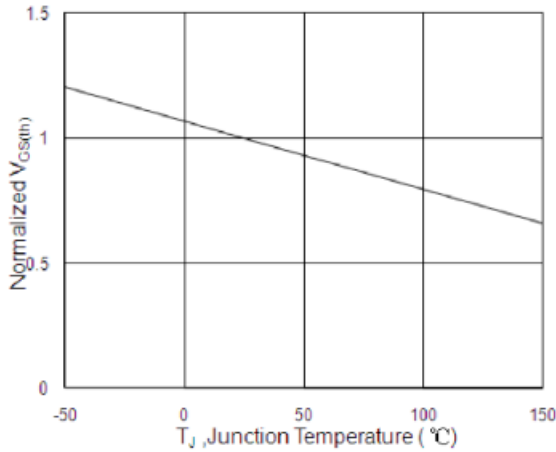


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

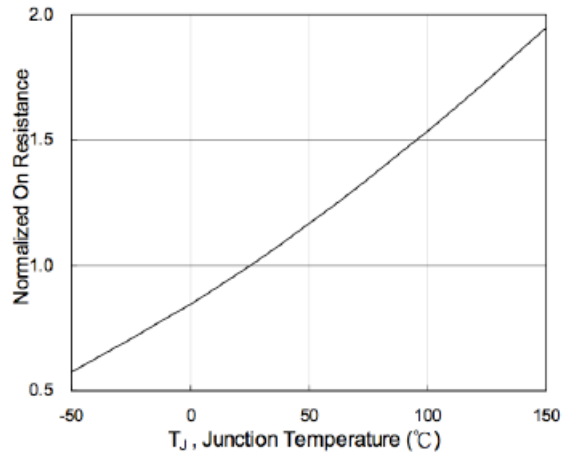


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

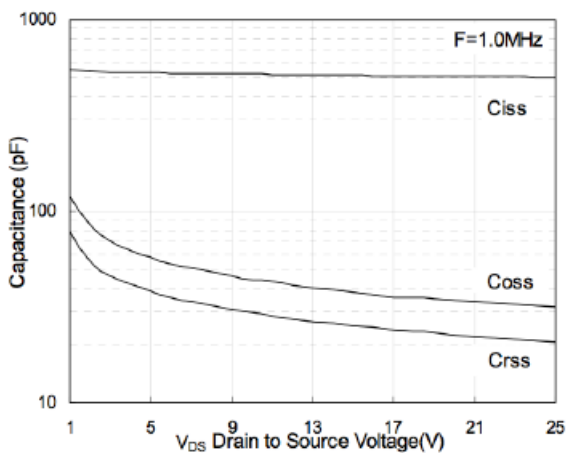


Fig.7 Capacitance

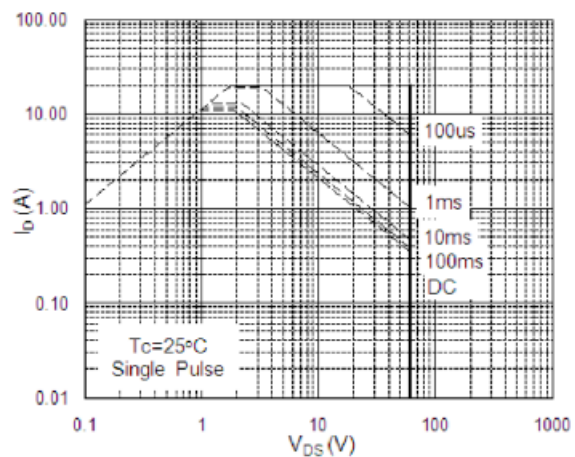


Fig.8 Safe Operating Area



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