



SPN4392W

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4392W is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

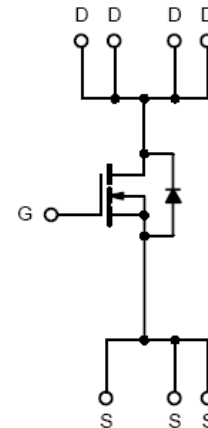
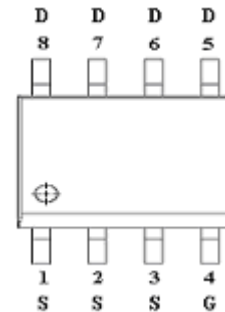
FEATURES

- ◆ 30V/13A, $R_{DS(ON)} = 8m\Omega @ V_{GS} = 10V$
- ◆ 30V/10A, $R_{DS(ON)} = 12m\Omega @ V_{GS} = 4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

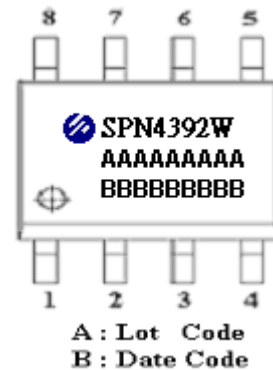
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- High-Side DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOP – 8P)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4392WS8RGB	SOP- 8P	SPN4392W

※ SPN4392WS8RGB : 13" Tape Reel ; Pb – Free; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	30	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	13	A
		TA=70°C	10	
Pulsed Drain Current	I _{DM}	50	A	
Continuous Source Current(Diode Conduction)	I _S	5.6	A	
Power Dissipation	P _D	TA=25°C	2.5	W
		TA=70°C	1.6	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	80	°C/W	



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ELECTRICAL CHARACTERISTICS

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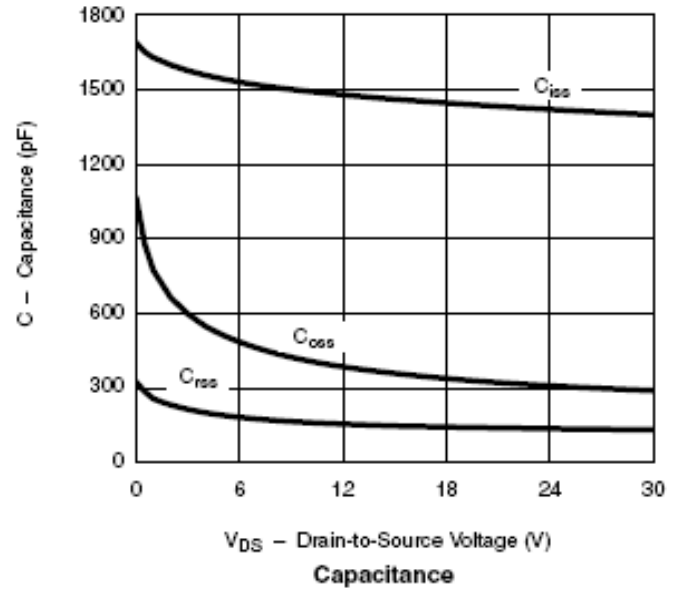
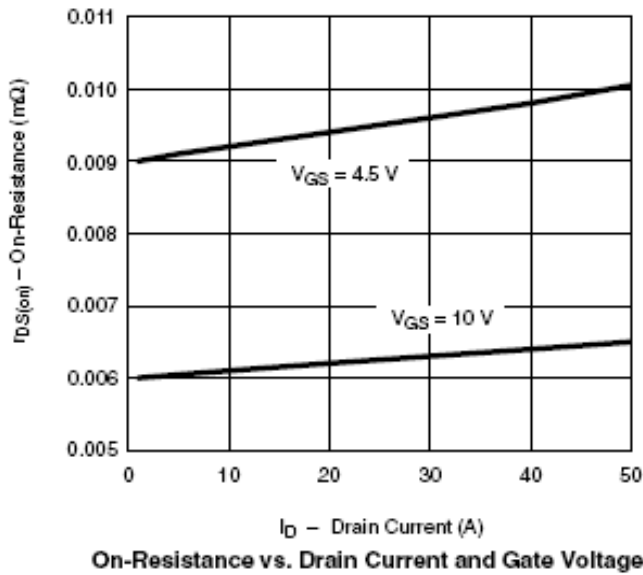
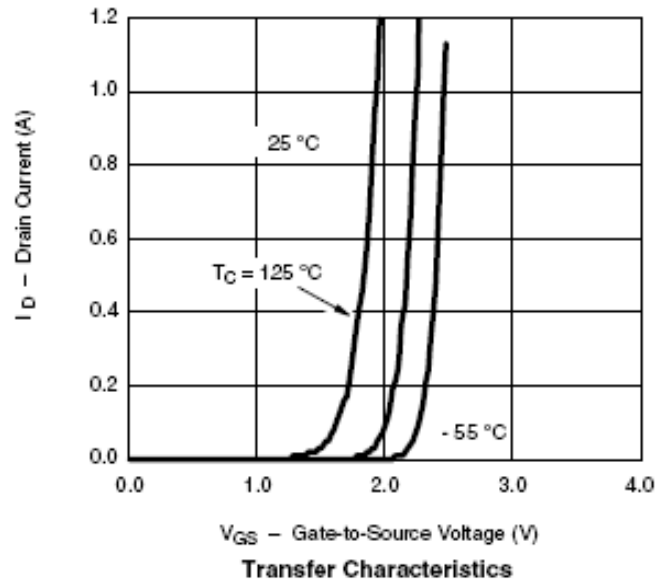
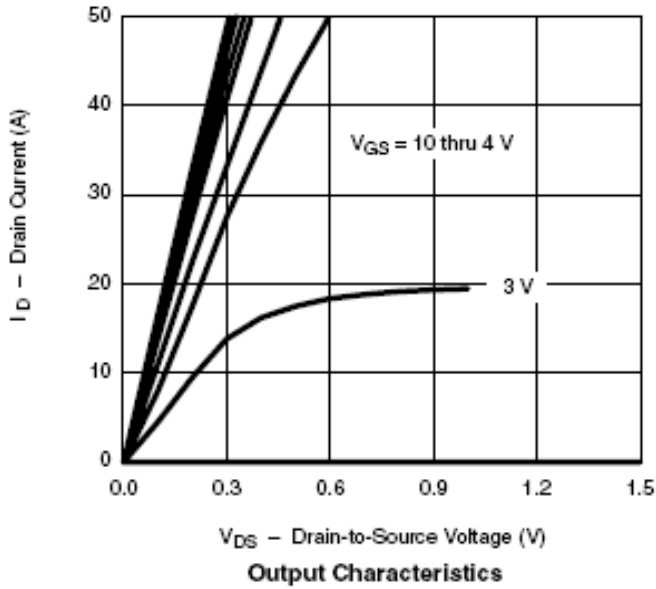
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _{DS} = 250uA	1.0		2.0	
Gate Leakage Current	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	uA
		V _{DS} = 24V, V _{GS} = 0V, T _J = 55C			100	
Drain-Source On-Resistance	R _{DSON}	V _{GS} = 10V, I _D = 13A		0.006	0.008	Ω
		V _{GS} = 4.5V, I _D = 10A		0.009	0.012	
Forward Transconductance	g _{fs}	V _{DS} = 15V, I _D = 20 A	10			S
Diode Forward Voltage	V _{SD}	I _F = 13 A, V _{GS} = 0V		1.0	1.5	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} = 15V, V _{GS} = 5V, I _D = 13 A		12	20	nC
Gate-Source Charge	Q _{gs}			4		
Gate-Drain Charge	Q _{gd}			5		
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, F=1MHz		1500		pF
Output Capacitance	C _{oss}			320		
Reverse Transfer Capacitance	C _{rss}			200		
Turn-On Time	t _{d(on)}	(V _{DD} = 15 V, I _D = 13 A, V _{GS} = 10V, R _G = 2.5Ω)		8	12	ns
	t _r			10	15	
Turn-Off Time	t _{d(off)}			18	30	
	t _f			6	9	



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TYPICAL CHARACTERISTICS

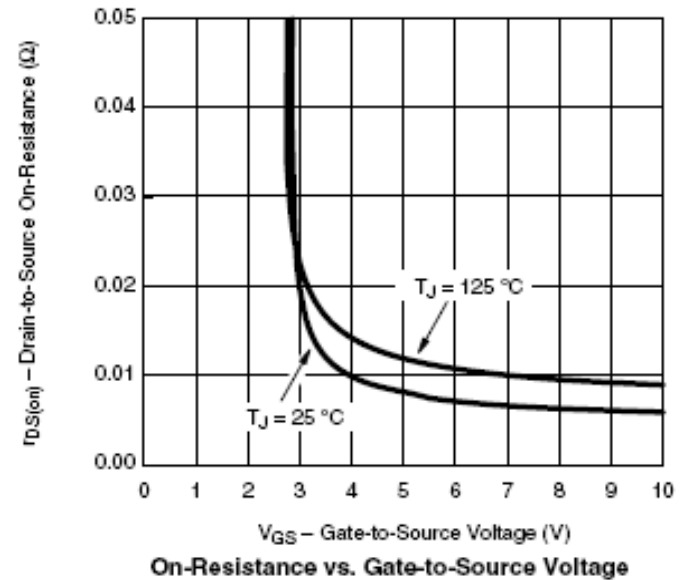
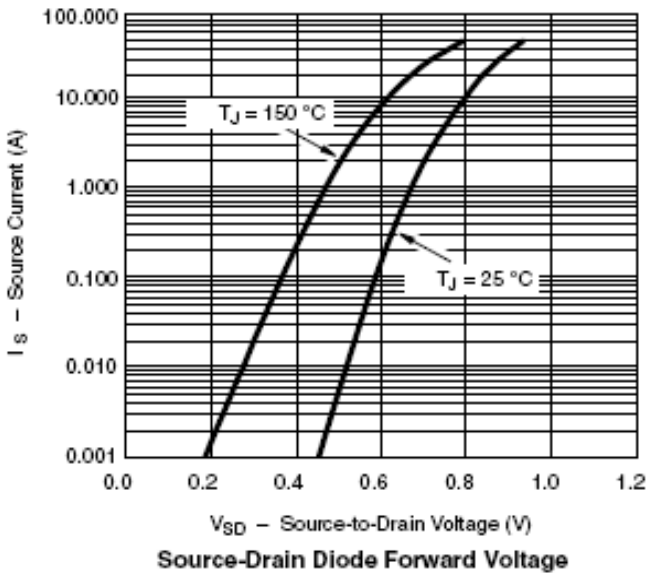
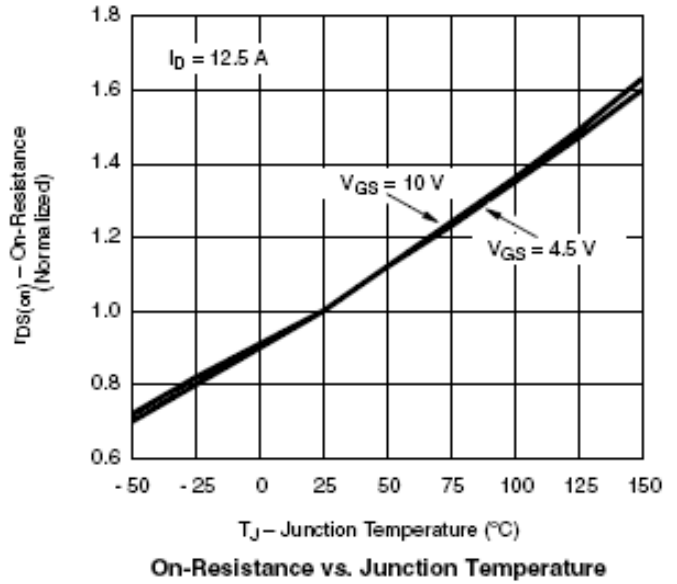
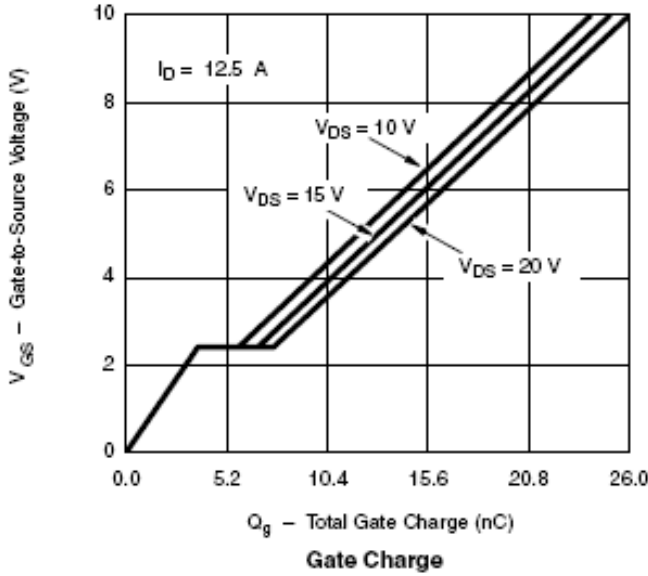




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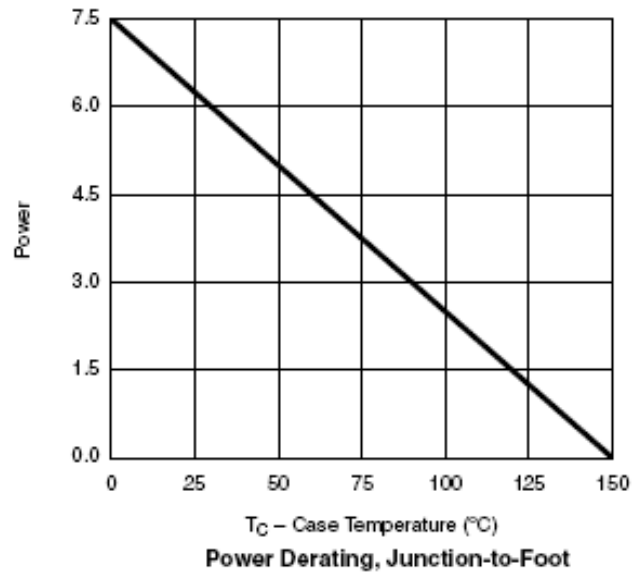
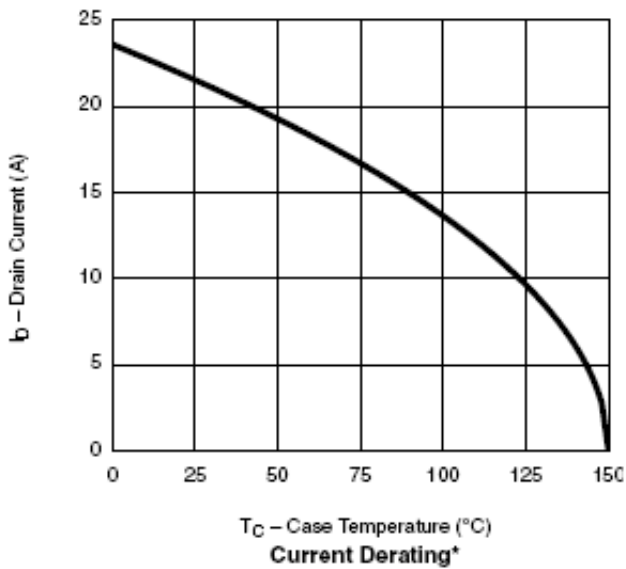
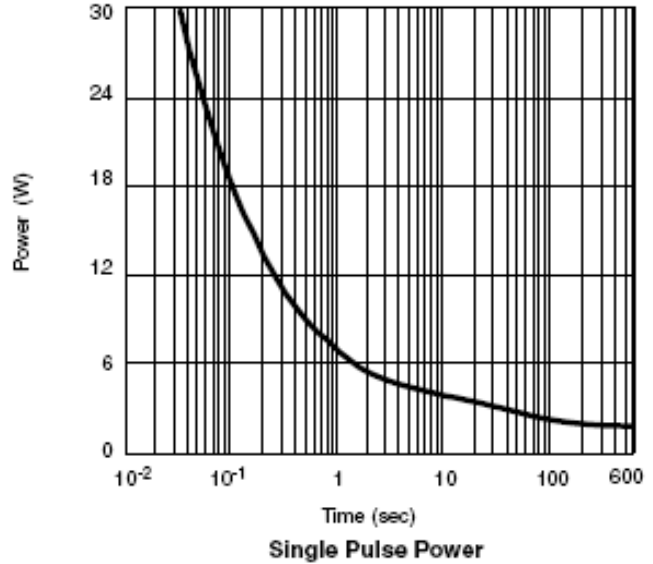
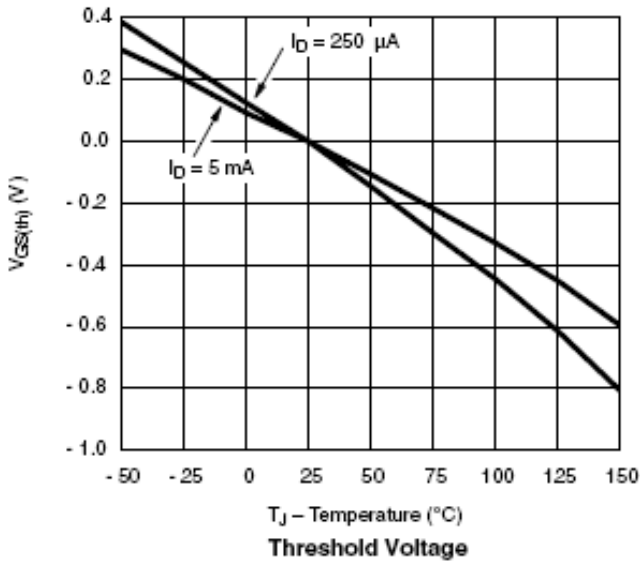




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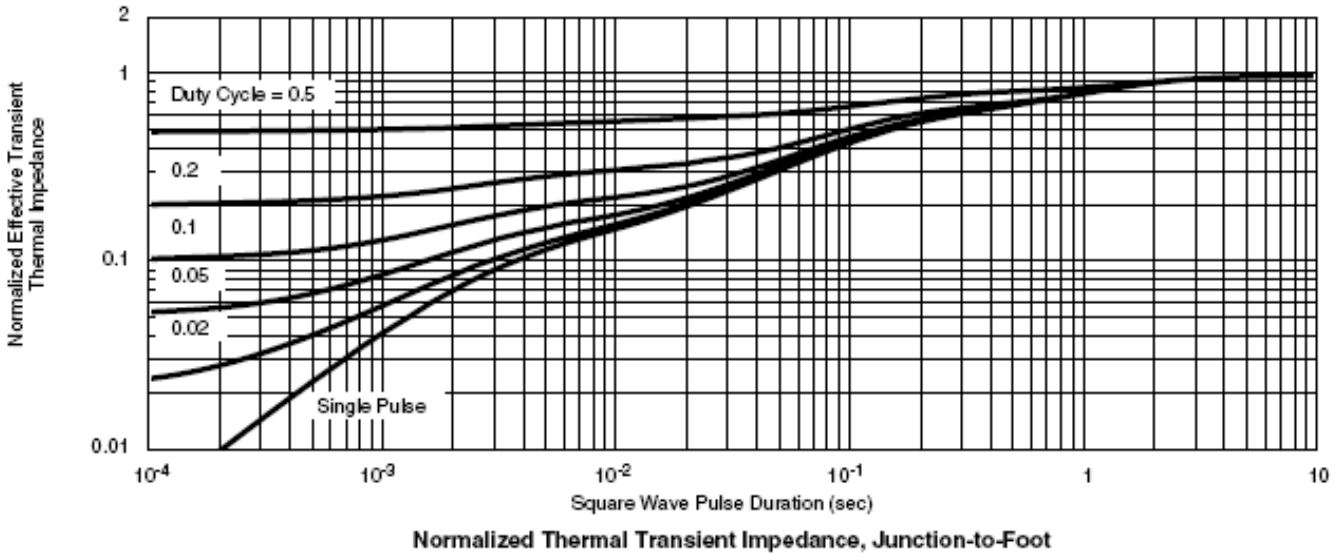
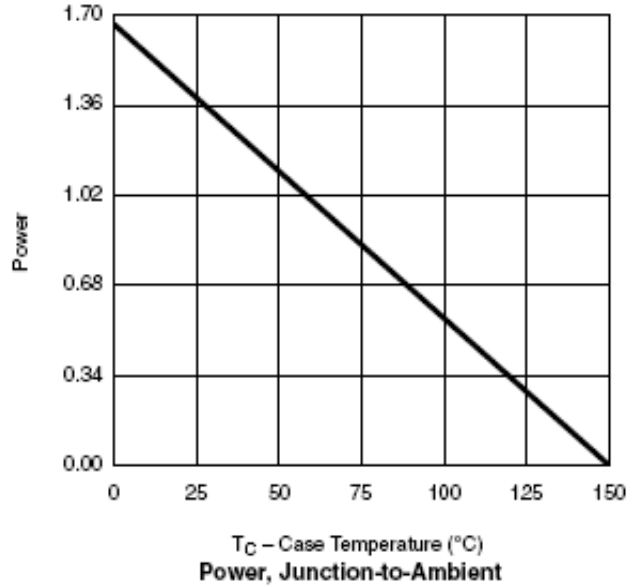
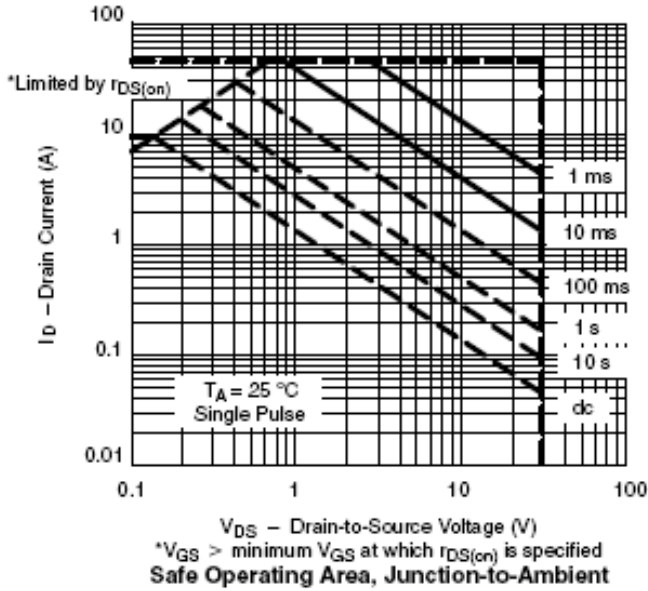




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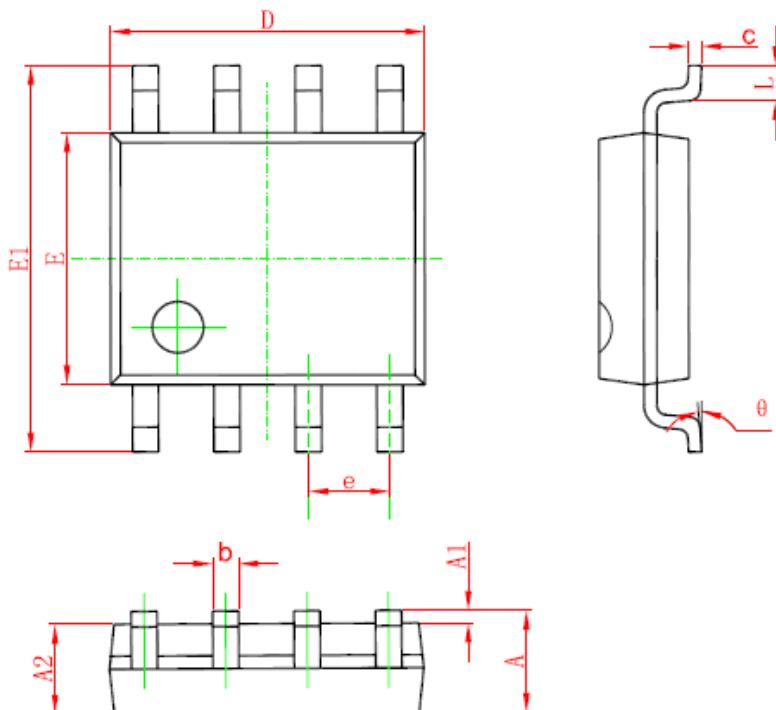




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SOP- 8 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



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