



SPN4394

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4394 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN4394 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

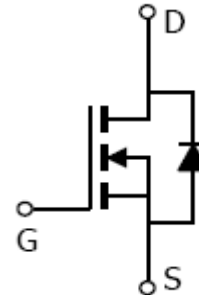
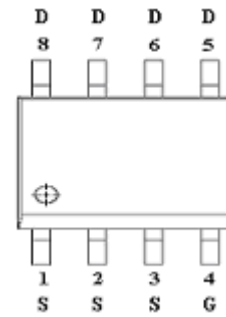
- ◆ 30V/12A, $R_{DS(ON)}=10.5m\Omega@V_{GS}=10V$
- ◆ 30V/12A, $R_{DS(ON)}=13.5m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

APPLICATIONS

- High Frequency Synchronous Buck Converter
- DC/DC Power System
- Load Switch

PIN CONFIGURATION

SOP-8



PART MARKING





SPN4394

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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4394S8RGB	SOP-8	SPN4394

※ SPN4394S8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V_{DSS}	30	V	
Gate –Source Voltage	V_{GSS}	± 20	V	
Continuous Drain Current	I_D	$T_A=25^{\circ}\text{C}$	12	A
		$T_A=70^{\circ}\text{C}$	9.5	
Pulsed Drain Current	I_{DM}	40	A	
Avalanche Current	I_{AS}	20	A	
Power Dissipation	P_D	2.5	W	
Operating Junction Temperature	T_J	150	$^{\circ}\text{C}$	
Storage Temperature Range	T_{STG}	-55/150	$^{\circ}\text{C}$	
Thermal Resistance-Junction to Ambient ($t \leq 10\text{s}$)	$R_{\theta JA}$	50	$^{\circ}\text{C}/\text{W}$	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=0V$			1	uA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ C$			5	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=12A$		9	10.5	mΩ
		$V_{GS}=4.5V, I_D=12A$		11	13.5	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=30A$		42		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=4.5V$ $I_D=12A$		10.6		nC
Gate-Source Charge	Q_{gs}			4.2		
Gate-Drain Charge	Q_{gd}			4		
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		1127		pF
Output Capacitance	C_{oss}			194		
Reverse Transfer Capacitance	C_{rss}			78		
Turn-On Time	$t_{d(on)}$	$V_{DD}=15V,$ $I_D=12A, V_{GEN}=10V$ $R_G=3.3\Omega$		6.4	13	nS
	t_r			70	127	
Turn-Off Time	$t_{d(off)}$			22.5	45	
	t_f			8	18	



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TYPICAL CHARACTERISTICS

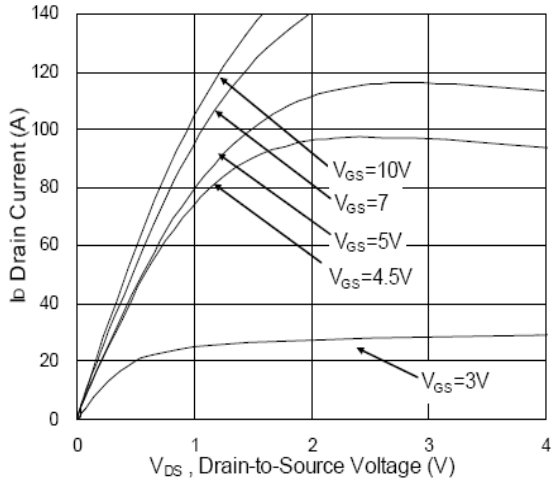


Fig. 1 Typical Output Characteristics

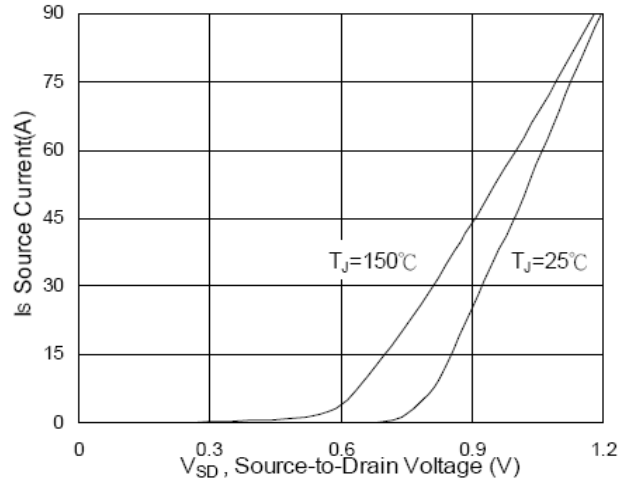


Fig. 2 Transfer Characteristics

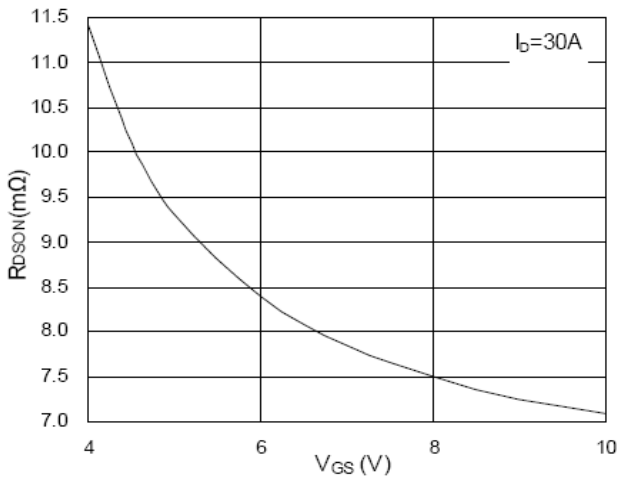


Fig. 3 On-Resistance vs Gate voltage

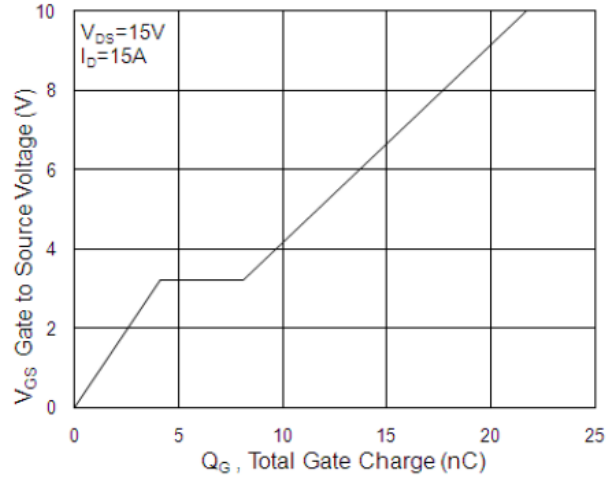


Fig. 4 Gate Charge Characteristics

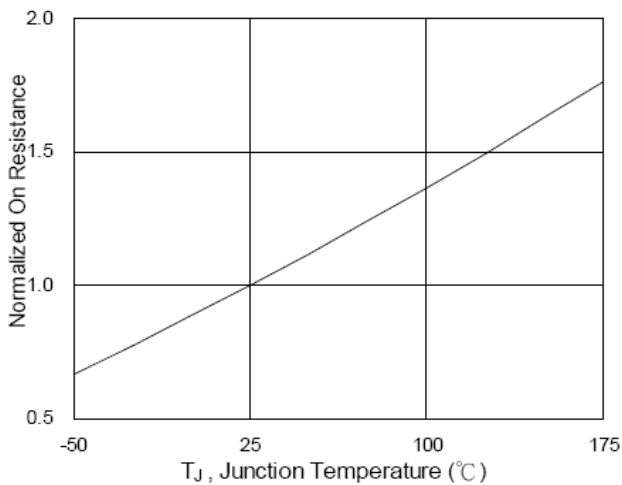


Fig. 5 On-Resistance vs Junction Temp

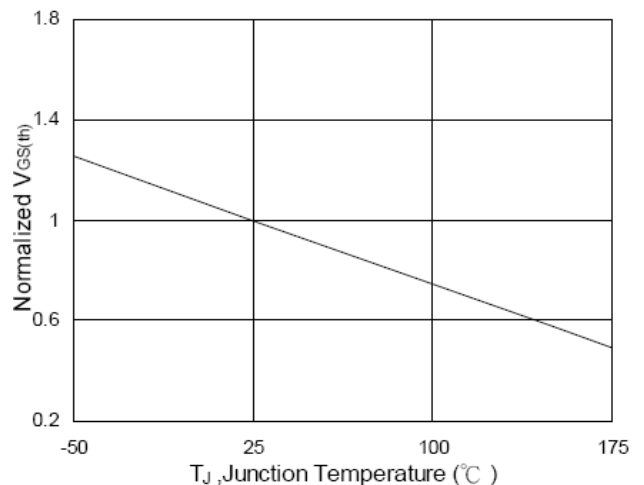


Fig. 6 Vgs vs Junction Temperature



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TYPICAL CHARACTERISTICS

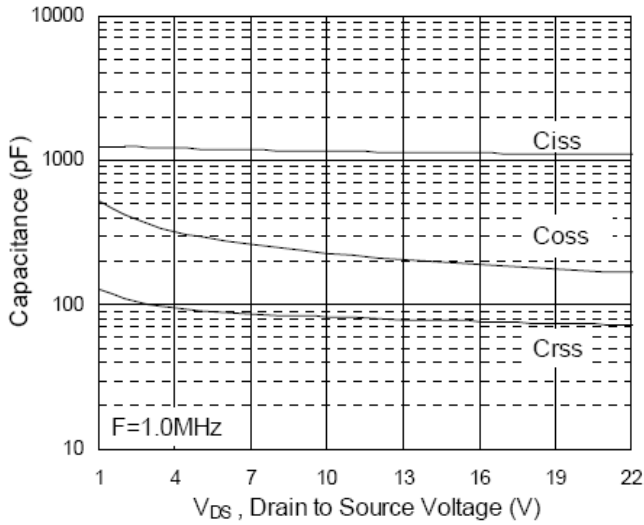


Fig. 7 Typical Capacitance Characteristics

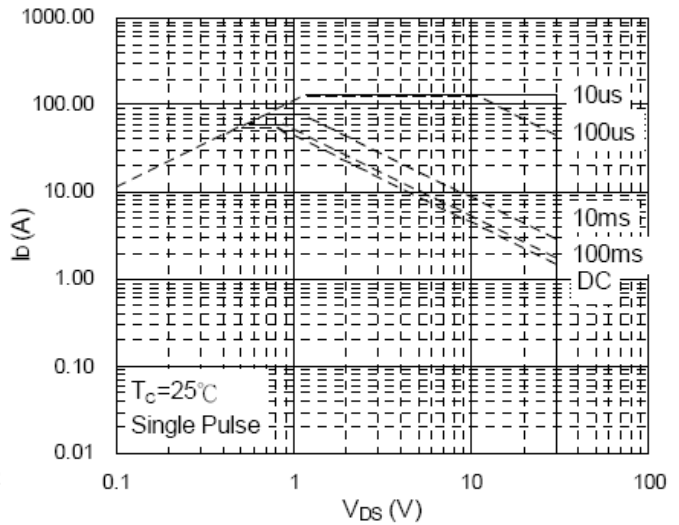


Fig. 8 Maximum Safe Operation Area

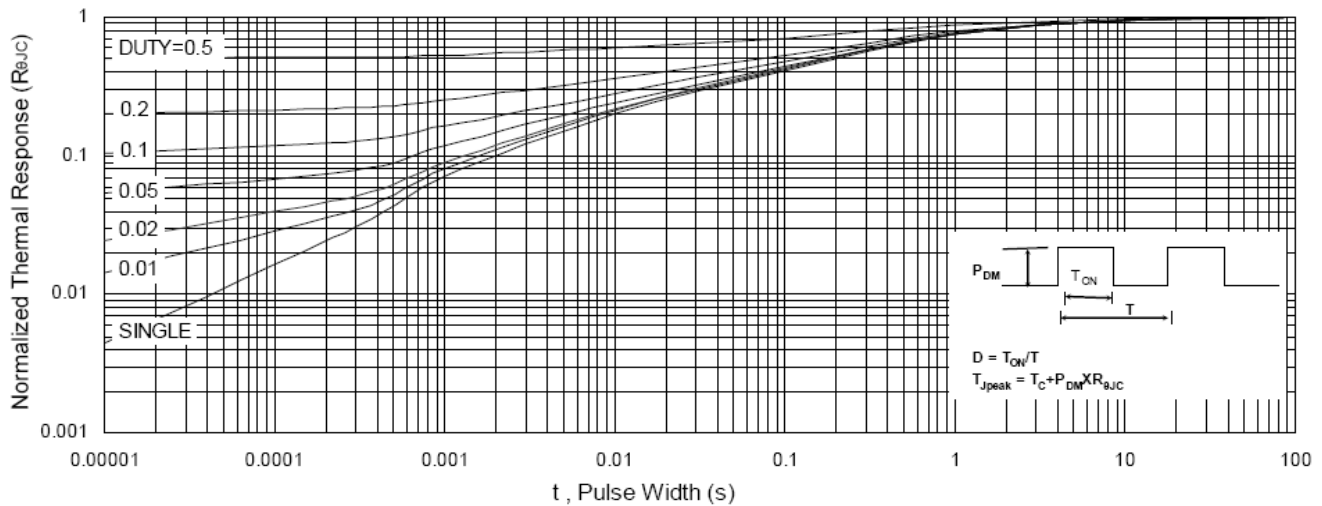


Fig. 9 Effective Transient Thermal Impedance

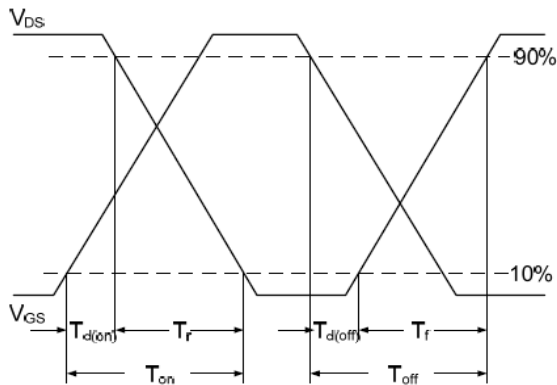


Fig. 10 Switching Time Waveform

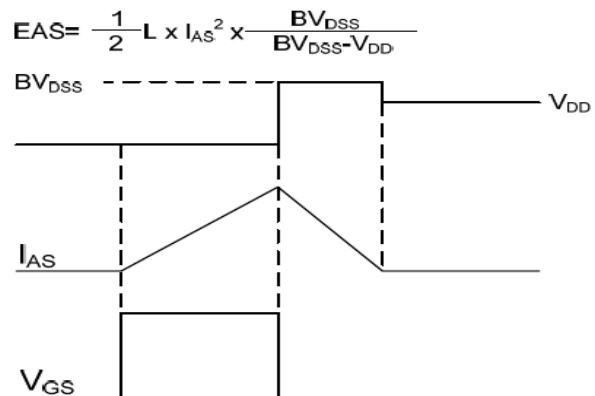


Fig. 11 Unclamped Inductive Waveform



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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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