



SPN4810

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4810 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

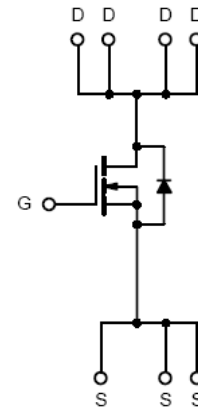
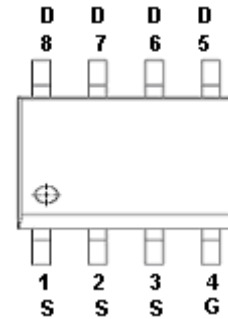
FEATURES

- ◆ 100V/14A, $R_{DS(ON)}=8.5m\Omega@V_{GS}=10V$
- ◆ 100V/10A, $R_{DS(ON)}=10.5m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

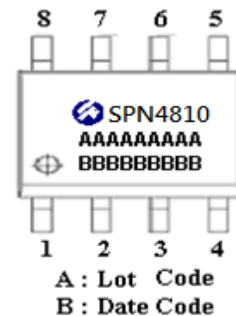
APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

PIN CONFIGURATION(SOP-8)



PART MARKING





SPN4810

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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4810S8RGB	SOP-8	SPN4810

※ SPN4810S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	100	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	14	A
		TA=70°C	8.9	
Pulsed Drain Current	I _{DM}	80	A	
Avalanche Energy, Single Pulse (L=0.1mH , Tc=25°C)	E _{AS}	80	mJ	
Power Dissipation	P _D	TA=25°C	3.1	W
		TA=70°C	2.2	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient (t ≤ 10s)	R _{θJA}	40	°C/W	
Thermal Resistance-Junction to Ambient (steady state)		75		



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.4	1.9	2.4	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$ $T_J=25^\circ C$			1	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=100^\circ C$			100	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=14A$		7.1	8.5	mΩ
		$V_{GS}=4.5V, I_D=10A$		8.4	10.5	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=14A$		70		S
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}=Open,$ $f=1MHz$		1.5		Ω
Diode Forward Voltage	V_{SD}	$I_S=14A, V_{GS}=0V$		0.9	1.2	V
Dynamic						
Total Gate Charge	$Q_g(10V)$	$V_{DS}=50V, V_{GS}=10V$ $I_D=14A$		49		nC
Total Gate Charge	$Q_g(4.5V)$			21		
Gate-Source Charge	Q_{gs}			8		
Gate-Drain Charge	Q_{gd}			7		
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V$ $f=1MHz$		3350		pF
Output Capacitance	C_{oss}			270		
Reverse Transfer Capacitance	C_{rss}			15		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V,$ $I_D=14A, V_{GS}=10V$ $R_G=10\Omega$		10		nS
	t_r			5		
Turn-Off Time	$t_{d(off)}$			32		
	t_f			6		



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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

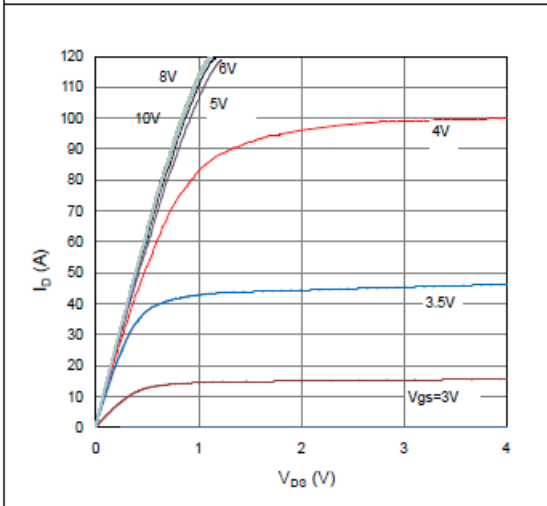


Figure 2. On-Resistance vs. Gate-Source Voltage

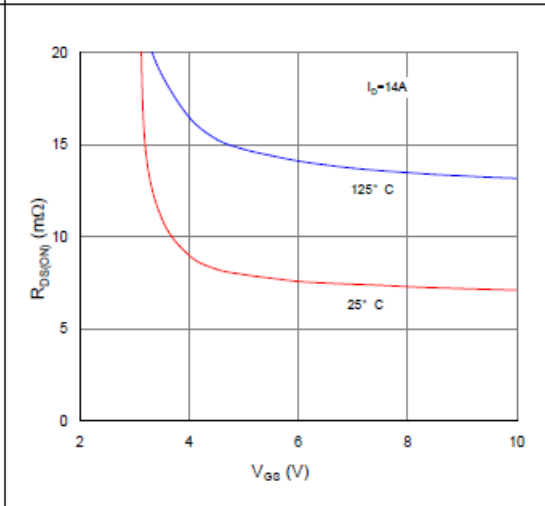


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

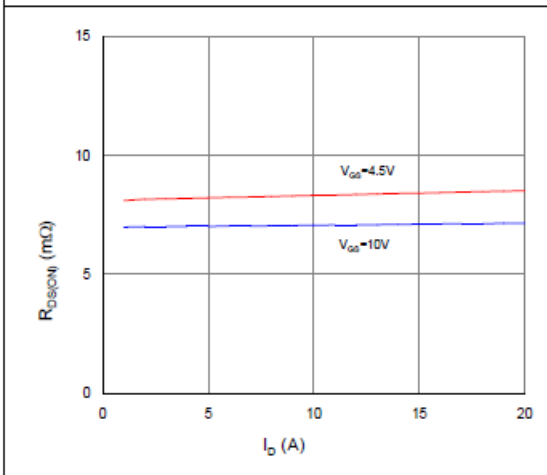


Figure 4. Normalized On-Resistance vs. Junction Temperature

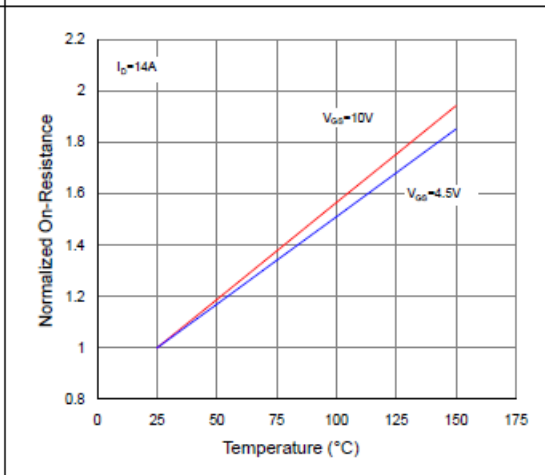


Figure 5. Typical Transfer Characteristics

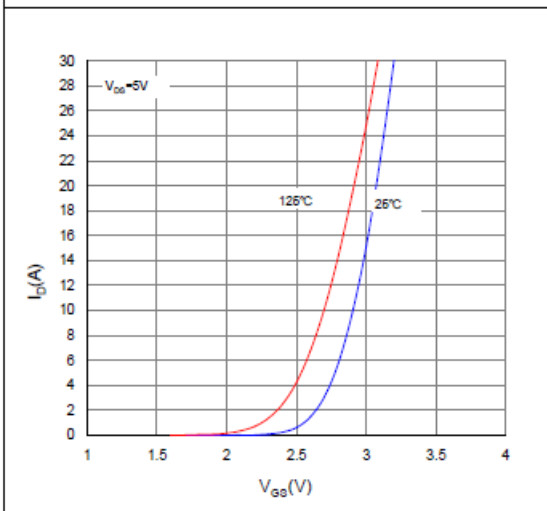
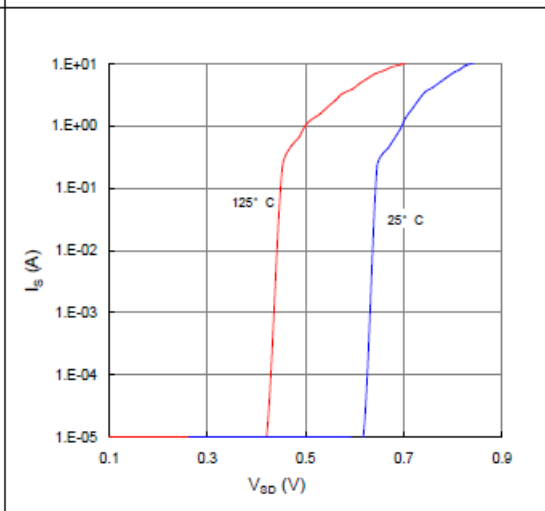


Figure 6. Typical Source-Drain Diode Forward Voltage





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TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

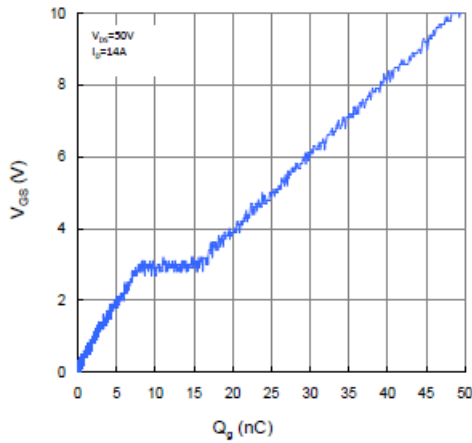


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

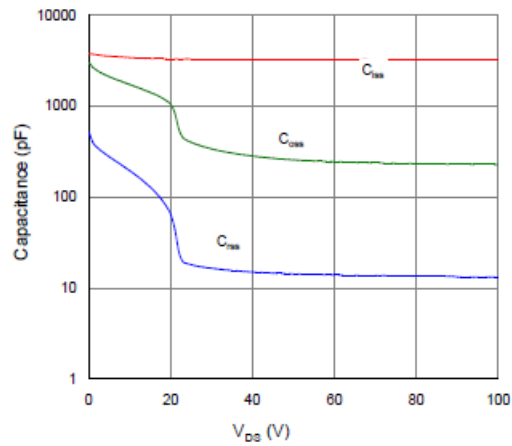


Figure 9. Maximum Safe Operating Area

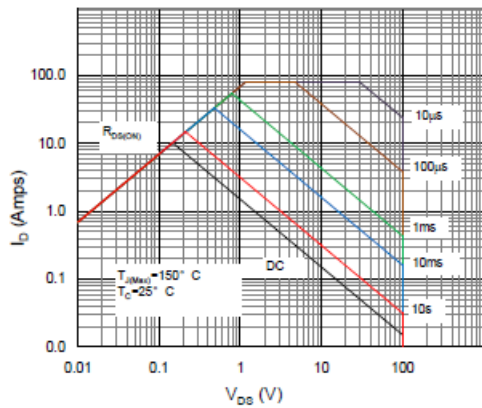


Figure 10. Maximum Drain Current vs. Case Temperature

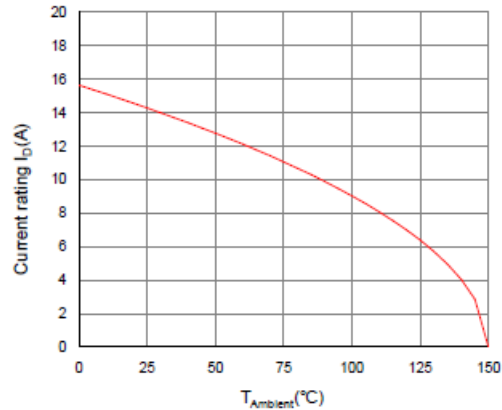
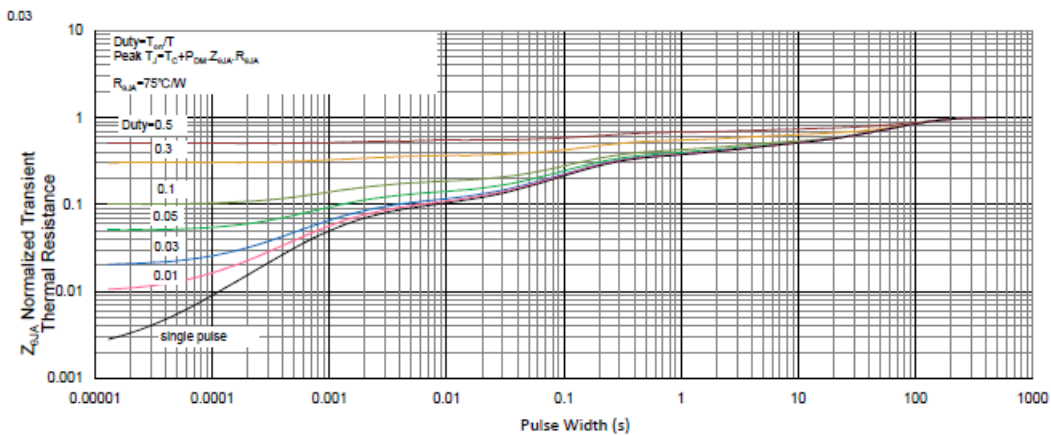


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





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