



# SPN4814A

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN4814A is the N-Channel enhancement mode power field effect transistors are produced using high cell density DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

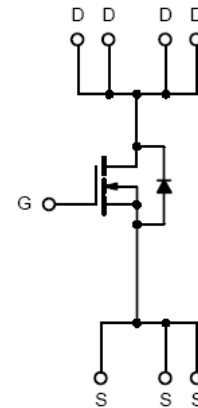
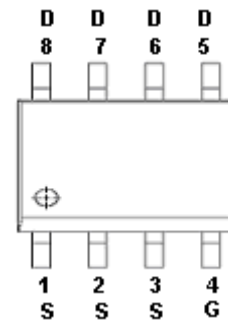
### FEATURES

- ◆ 100V/20A,  $R_{DS(ON)}=10.5m\Omega@V_{GS}=10V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

### APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

### PIN CONFIGURATION(SOP-8)



### PART MARKING





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### PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4814AS8RGB	SOP-8	SPN4814A

※ SPN4814AS8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	100	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>C</sub> =25°C	13	A
		T <sub>C</sub> =100°C	8	
Pulsed Drain Current	I <sub>DM</sub>	120	A	
Avalanche Energy, Single Pulse (L=0.1mH , T <sub>C</sub> =25°C)	E <sub>AS</sub>	31	mJ	
Power Dissipation	P <sub>D</sub>	3.1	W	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Case	R <sub>θJC</sub>	0.85	°C/W	
Thermal Resistance-Junction to Ambient (steady state)	R <sub>θJA</sub>	75		



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	3.0	4.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$ $T_J=25^\circ C$			1	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=100^\circ C$			100	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		9.4	10.5	mΩ
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=20A$		39		S
Gate Resistance	$R_G$	$V_{GS}=0V, V_{DS}=\text{Open},$ $f=1\text{MHz}$		1.5		Ω
Diode Forward Voltage	$V_{SD}$	$I_S=20A, V_{GS}=0V$		0.9	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=50V, V_{GS}=10V$ $I_D=20A$		23.0		nC
Gate-Source Charge	$Q_{gs}$			5.5		
Gate-Drain Charge	$Q_{gd}$			6.5		
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V$ $f=1\text{MHz}$		1326		pF
Output Capacitance	$C_{oss}$			262		
Reverse Transfer Capacitance	$C_{rss}$			7.7		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V,$ $I_D=20A, V_{GS}=10V$ $R_G=10\Omega$		6		nS
	$t_r$			3		
Turn-Off Time	$t_{d(off)}$			17		
	$t_f$			4		



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## TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

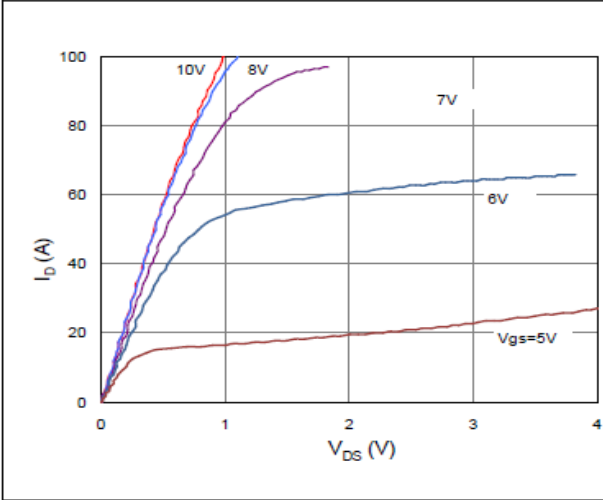


Figure 2. On-Resistance vs. Gate-Source Voltage

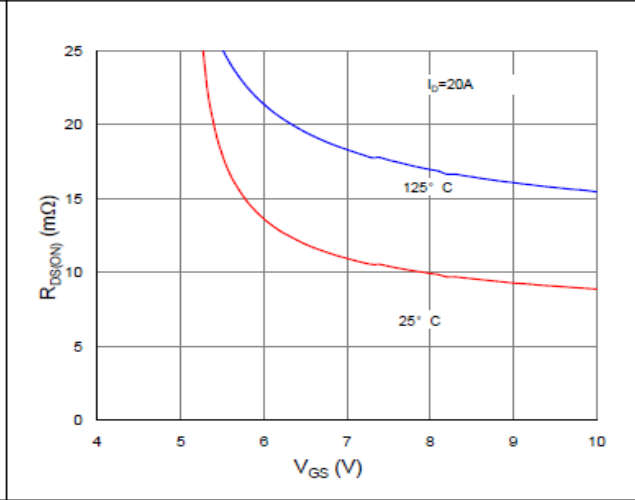


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

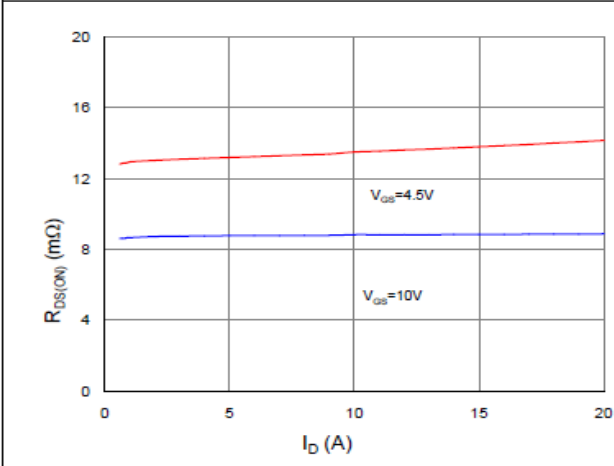


Figure 4. Normalized On-Resistance vs. Junction Temperature

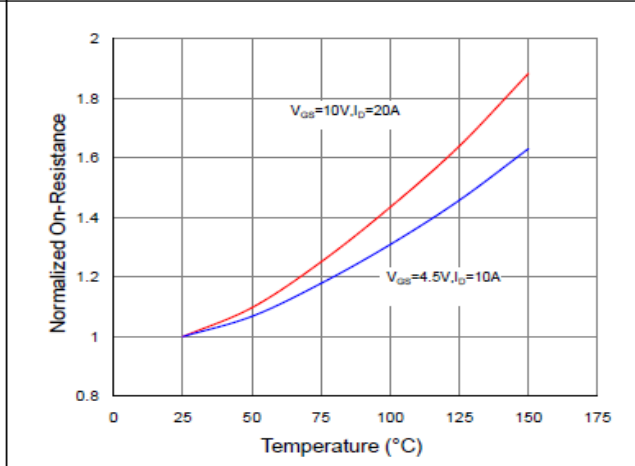


Figure 5. Typical Transfer Characteristics

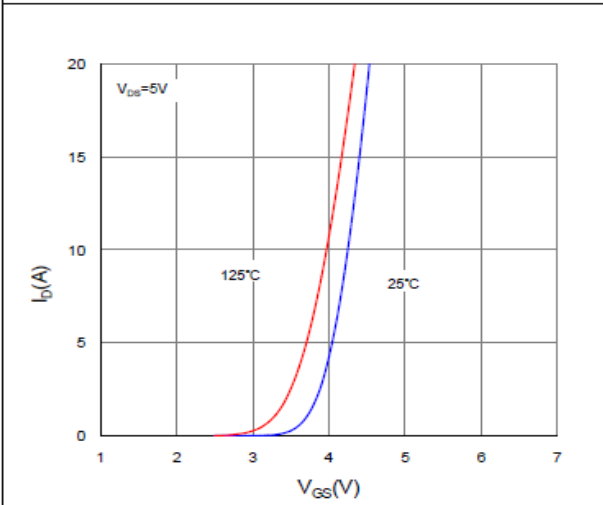
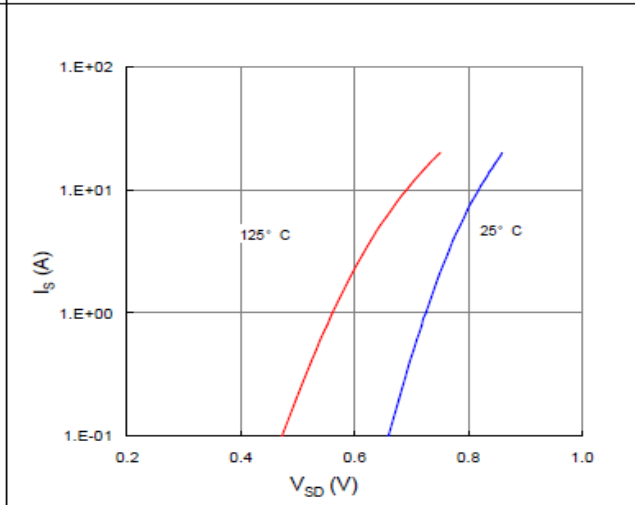


Figure 6. Typical Source-Drain Diode Forward Voltage





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## TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

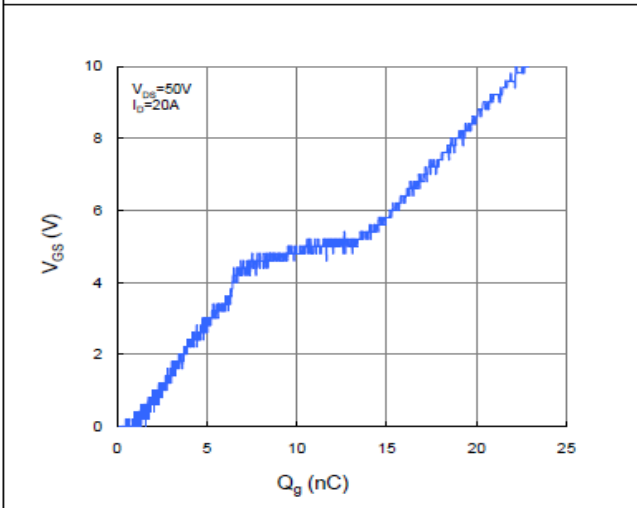


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

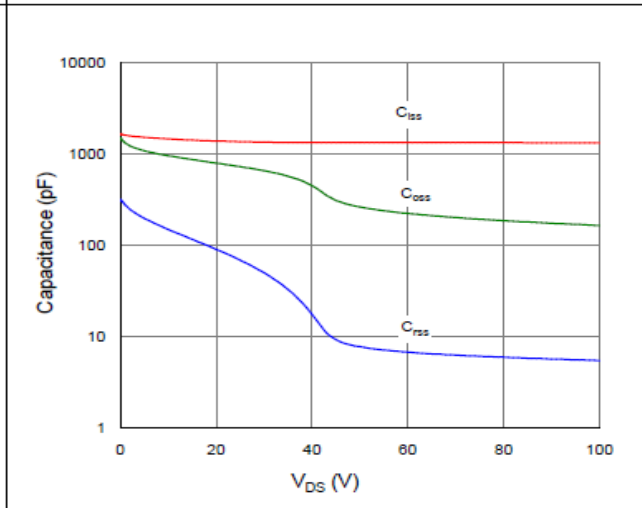


Figure 9. Maximum Safe Operating Area

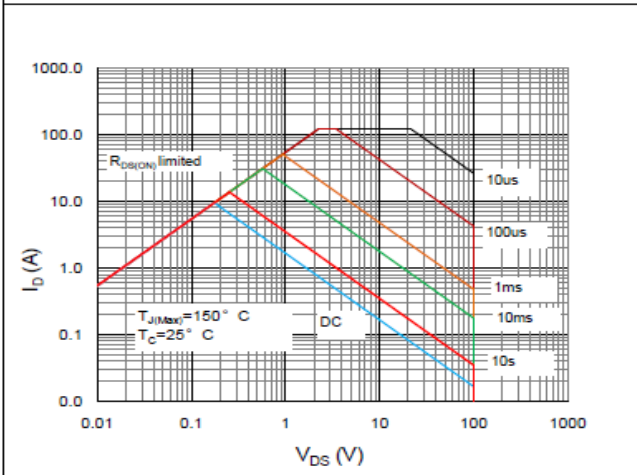


Figure 10. Maximum Drain Current vs. Case Temperature

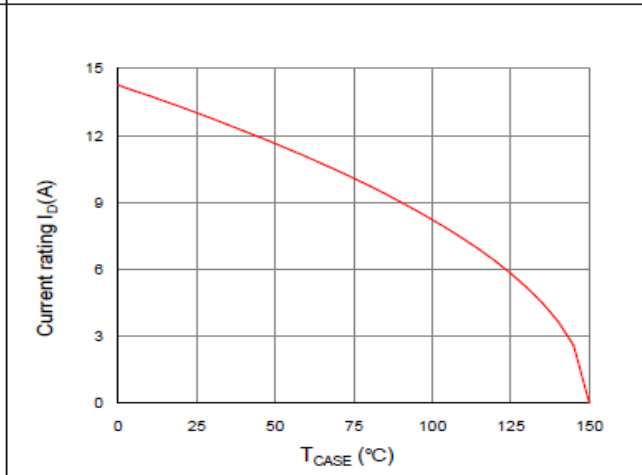
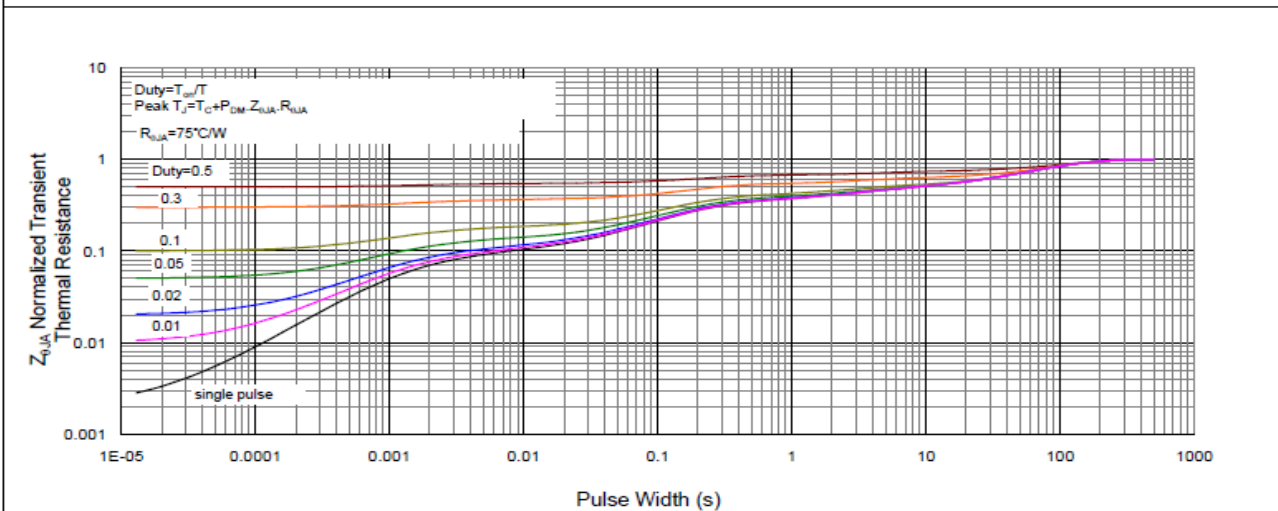


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case





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