



SPN4842

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4842 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching .

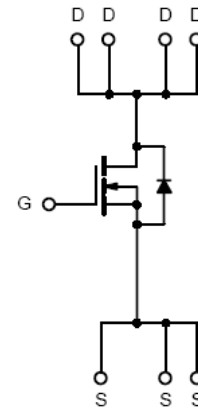
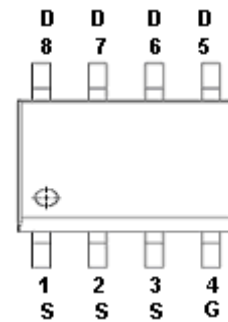
FEATURES

- ◆ 45V/6A, $R_{DS(ON)}=8m\Omega@V_{GS}=10V$
- ◆ 45V/3A, $R_{DS(ON)}=12m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- Charger Adapter
- LED Lighting

PIN CONFIGURATION(SOP – 8P)



PART MARKING





SPN4842

N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4842S8RGB	SOP-8P	SPN4842

※ SPN4842S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	45	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current	I _D	TA=25°C	13.3
		TA=100°C	8.4
Pulsed Drain Current	I _{DM}	53.2	A
Single Pulse Avalanche Energy	E _{AS}	38	mJ
Avalanche Current	I _{AS}	27	A
Power Dissipation	P _D	TA=25°C	2.5
		TA=70°C	1.4
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	50	°C/W



SPN4842

N-Channel Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	45			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=45V, V_{GS}=0V, T_J=25^\circ C$			1	μA
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=6A$		6	8	m Ω
		$V_{GS}=4.5V, I_D=3A$		8	12	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=6A$		25		S
Diode Forward Voltage	V_{SD}	$I_S=13.3A, V_{GS}=0V$			1.5	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=20V, V_{GS}=10V$ $I_D=13.3A$		31.5		nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			9		
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1MHz$		1600		pF
Output Capacitance	C_{oss}			180		
Reverse Transfer Capacitance	C_{rss}			130		
Turn-On Time	$t_{d(on)}$	$V_{DD}=20V,$ $I_D=13.3A, V_{GS}=10V$ $R_G=6\Omega$		12		nS
	t_r			82		
Turn-Off Time	$t_{d(off)}$			33		
	t_f			59		
Gate resistance	R_g	$V_{GS}=0V, V_{DS}=0V, f=1MHz$		1.2		Ω

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. $V_{DD}=50V, V_{GS}=10V, L=0.1mH, I_{AS}=27A, R_G=25\Omega, \text{Starting } T_J=25^\circ C$
3. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
4. Essentially independent of operating temperature.



SPN4842 N-Channel Enhancement Mode MOSFET

TYPICAL CHARACTERISTICS

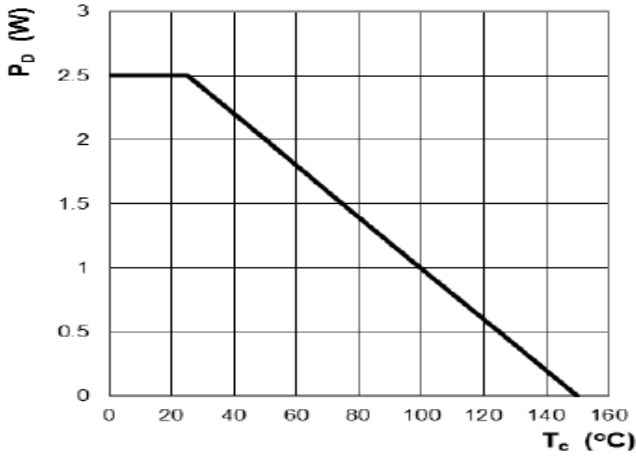


Figure 1: Power Dissipation

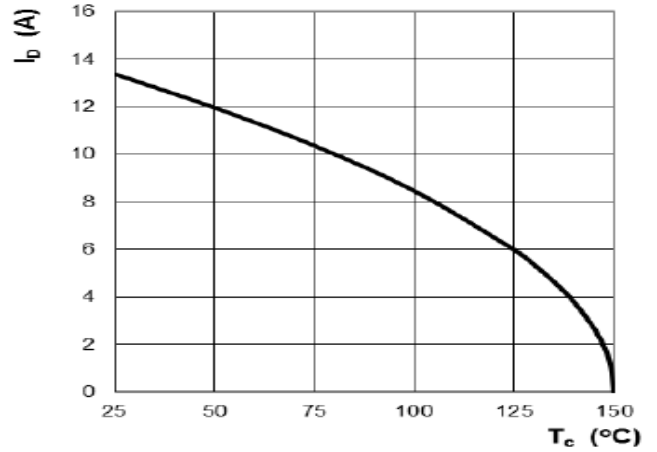


Figure 2: Continuous Drain Current vs. T_c

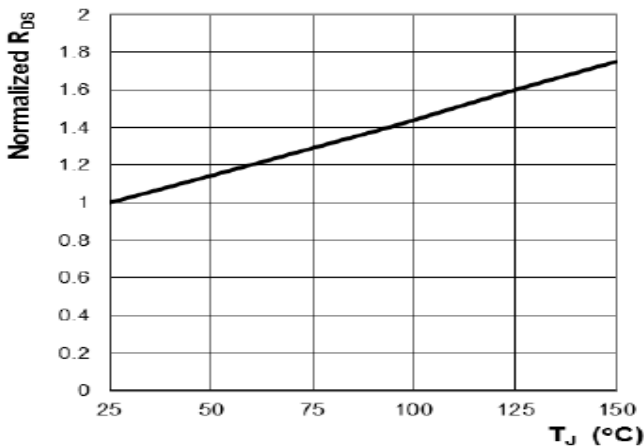


Figure 3: Normalized $R_{DS(on)}$ vs. T_j

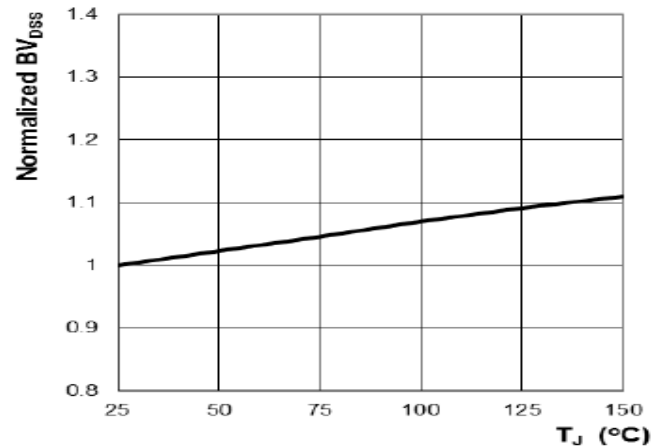


Figure 4: Normalized BV_{DSS} vs. T_j

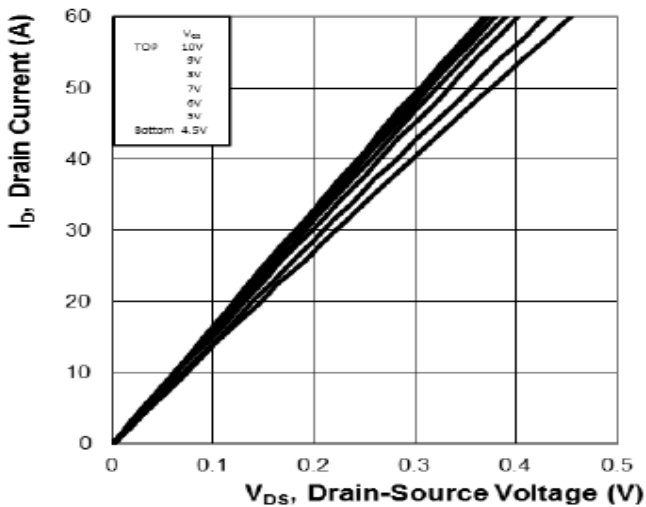


Figure 5: On-Region Characteristics

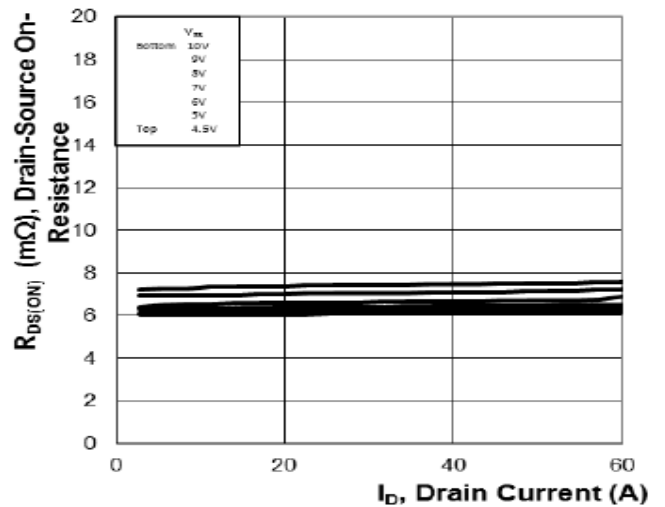


Figure 6: Typ. R_{DS} Variation vs. I_D and V_{GS}



SPN4842 N-Channel Enhancement Mode MOSFET

TYPICAL CHARACTERISTICS

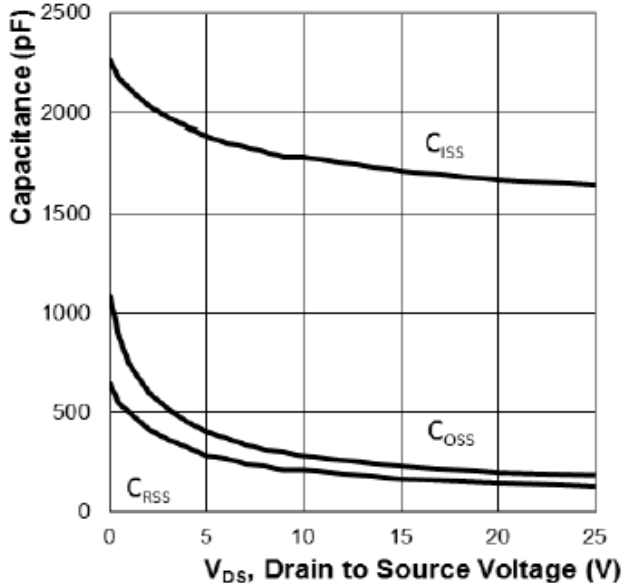


Figure 7: Typ. Capacitance Characteristics

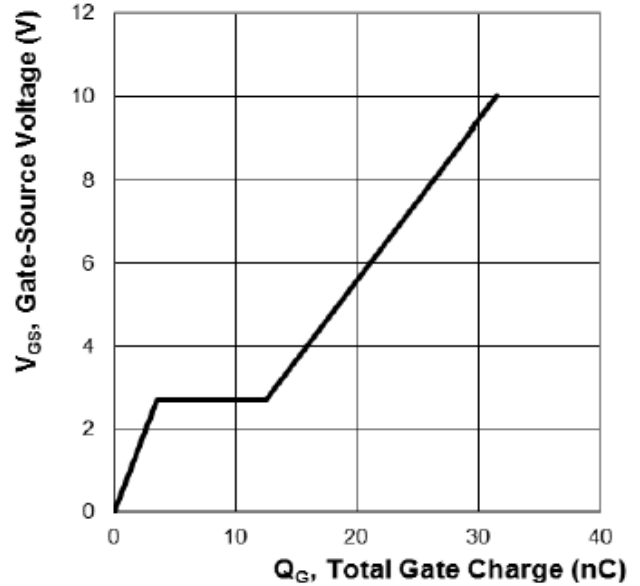


Figure 8: Typ. Gate Charge Characteristics

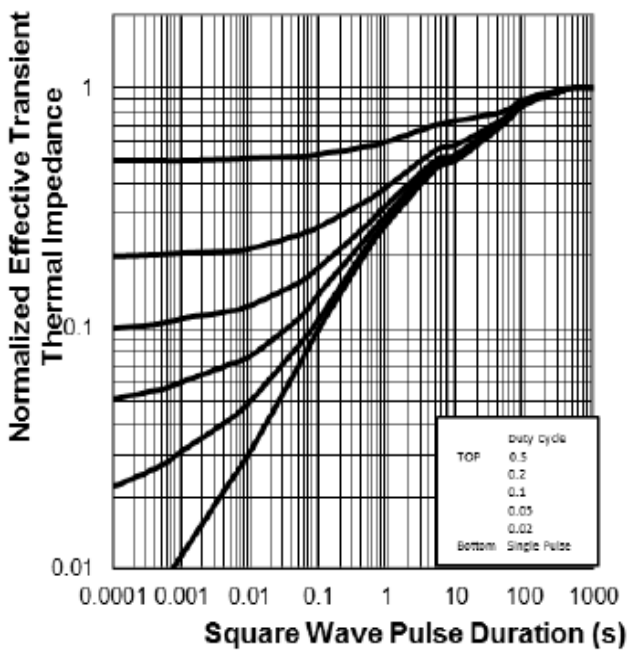


Figure 9: Normalized Thermal Transient Impedance, Junction-to-Case

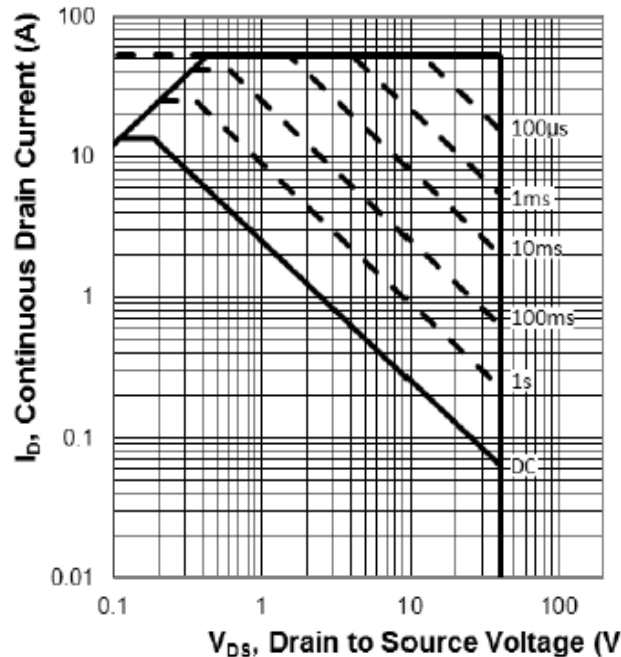


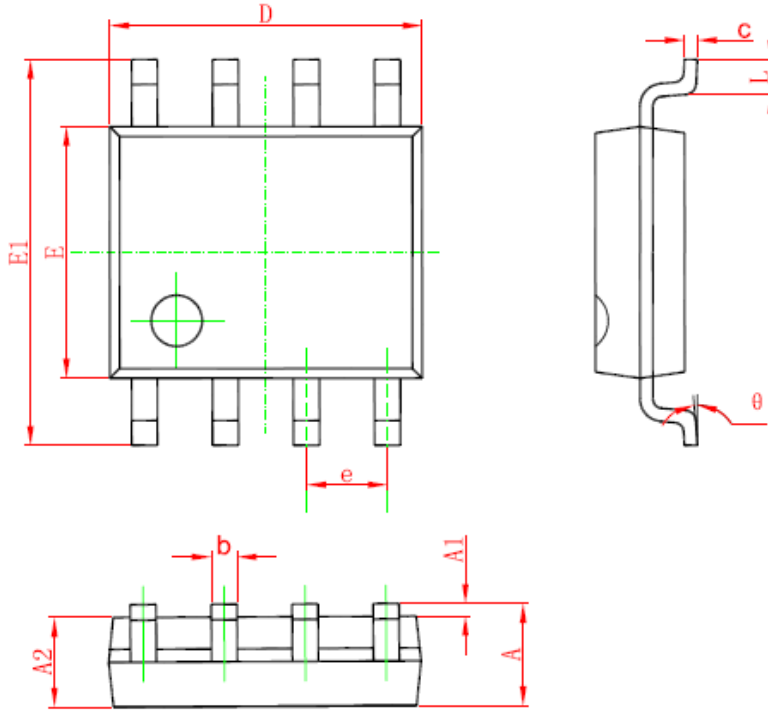
Figure 10: Maximum Safe Operation Area



SPN4842

N-Channel Enhancement Mode MOSFET

SOP- 8 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°



SPN4842

N-Channel Enhancement Mode MOSFET

Information provided is alleged to be exact and consistent. SYNC Power Corporation presumes no responsibility for the penalties of use of such information or for any violation of patents or other rights of third parties which may result from its use. No license is granted by allegation or otherwise under any patent or patent rights of SYNC Power Corporation. Conditions mentioned in this publication are subject to change without notice. This publication surpasses and replaces all information previously supplied. SYNC Power Corporation products are not authorized for use as critical components in life support devices or systems without express written approval of SYNC Power Corporation.

© The SYNC Power logo is a registered trademark of SYNC Power Corporation

© 2017 SYNC Power Corporation – Printed in Taiwan – All Rights Reserved

SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

© <http://www.syncpower.com>