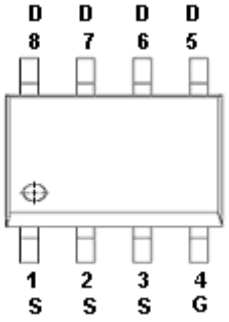
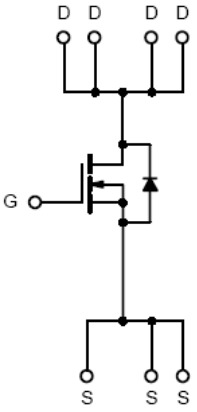
# SPN4842
## N-Channel Enhancement Mode MOSFET

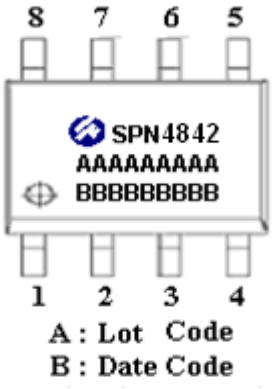
### DESCRIPTION
The SPN4842 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching .

### APPLICATIONS
- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- Charger Adapter
- LED Lighting

### FEATURES
- 45V/6A,$R_{DS(ON)}$=9.5mΩ@$V_{GS}$=10V
- 45V/3A,$R_{DS(ON)}$=12.5mΩ@$V_{GS}$=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP – 8P package design

### PIN CONFIGURATION(SOP – 8P)



### PART MARKING


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**PIN DESCRIPTION**

| Pin | Symbol | Description |
|---|---|---|
| 1 | S | Source |
| 2 | S | Source |
| 3 | S | Source |
| 4 | G | Gate |
| 5 | D | Drain |
| 6 | D | Drain |
| 7 | D | Drain |
| 8 | D | Drain |

**ORDERING INFORMATION**

| Part Number | Package | Part Marking |
|---|---|---|
| SPN4842S8RGB | SOP-8P | SPN4842 |

※ SPN4842S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

**ABSOULTE MAXIMUM RATINGS**

($T_A$=25℃ Unless otherwise noted)

| Parameter | | Symbol | Typical | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | 45 | V |
| Gate –Source Voltage | | $V_{GSS}$ | ±20 | V |
| Continuous Drain Current | $T_A$=25℃ | $I_D$ | 13.3 | A |
| | $T_A$=100℃ | | 8.4 | |
| Pulsed Drain Current | | $I_{DM}$ | 53.2 | A |
| Single Pulse Avalanche Energy | | $E_{AS}$ | 38 | mJ |
| Avalanche Current | | $I_{AS}$ | 27 | A |
| Power Dissipation | $T_A$=25℃ | $P_D$ | 2.5 | W |
| | $T_A$=70℃ | | 1.4 | |
| Operating Junction Temperature | | $T_J$ | -55/150 | ℃ |
| Storage Temperature Range | | $T_{STG}$ | -55/150 | ℃ |
| Thermal Resistance-Junction to Ambient | | $R_{\theta JA}$ | 50 | ℃/W |

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**ELECTRICAL CHARACTERISTICS**

($T_A$=25℃ Unless otherwise noted)

| Parameter | Symbol | Conditions | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$=0V,$I_D$=250uA | 45 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250uA | 1.0 | | 2.5 | |
| Gate Leakage Current | $I_{GSS}$ | $V_{DS}$=0V,$V_{GS}$=±20V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=45V,$V_{GS}$=0V, $T_J$=25℃ | | | 1 | uA |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}$=10V,$I_D$=6A | | 6 | 9.5 | mΩ |
| | | $V_{GS}$=4.5V,$I_D$=3A | | 8 | 12.5 | |
| Forward Transconductance | gfs | $V_{DS}$=5V,$I_D$=6A | | 25 | | S |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=13.3A,$V_{GS}$ =0V | | | 1.5 | V |
| **Dynamic** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$=20V, $V_{GS}$=10V $I_D$=13.3A | | 31.5 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 3.5 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 9 | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=25V, $V_{GS}$=0V f=1MHz | | 1600 | | pF |
| Output Capacitance | $C_{oss}$ | | | 180 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 130 | | |
| Turn-On Time | $t_{d(on)}$ | $V_{DD}$=20V, $I_D$=13.3A,$V_{GS}$=10V $R_G$=6Ω | | 12 | | nS |
| | $t_r$ | | | 82 | | |
| Turn-Off Time | $t_{d(off)}$ | | | 33 | | |
| | $t_f$ | | | 59 | | |
| Gate resistance | $R_g$ | $V_{GS}$=0V,$V_{DS}$=0V, f=1MHz | | 1.2 | | Ω |

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. $V_{DD}$=50V, $V_{GS}$=10V, L=0.1mH , $I_{AS}$=27A , $R_G$=25Ω , Starting $T_J$=25℃
3. The data tested by pulsed, pulse width ≦300us, duty cycle ≦2%.
4. Essentially independent of operating temperature.

## TYPICAL CHARACTERISTICS

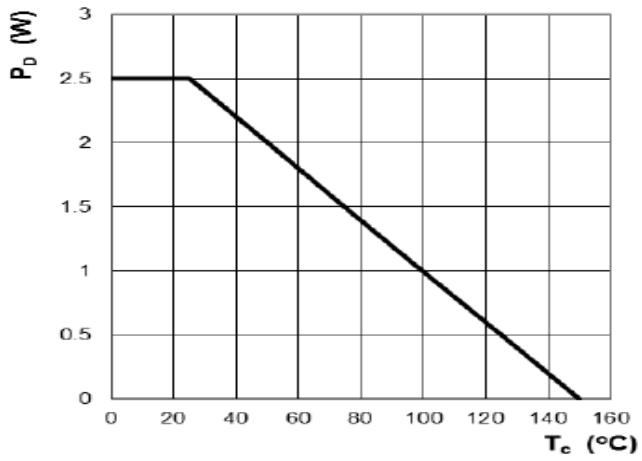



Figure 1: Power Dissipation

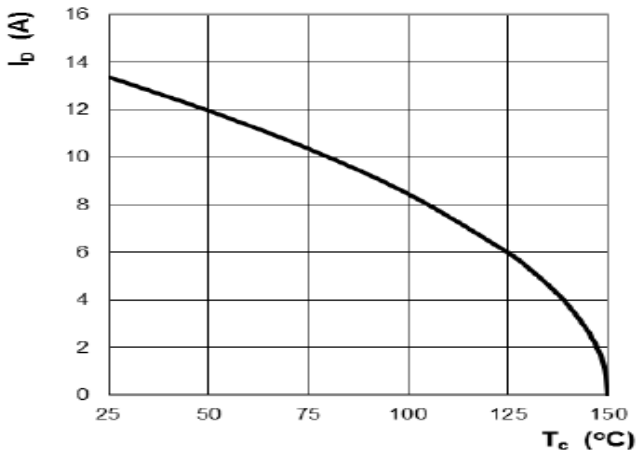



Figure 2: Continuous Drain Current vs. $T_C$

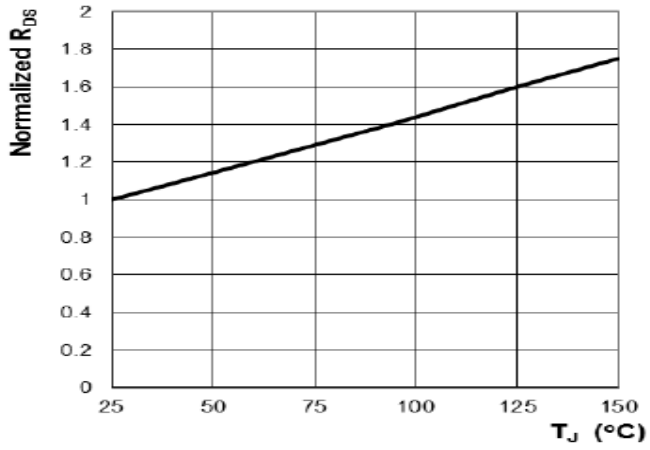



Figure 3: Normalized $R_{DS(ON)}$ vs. $T_J$

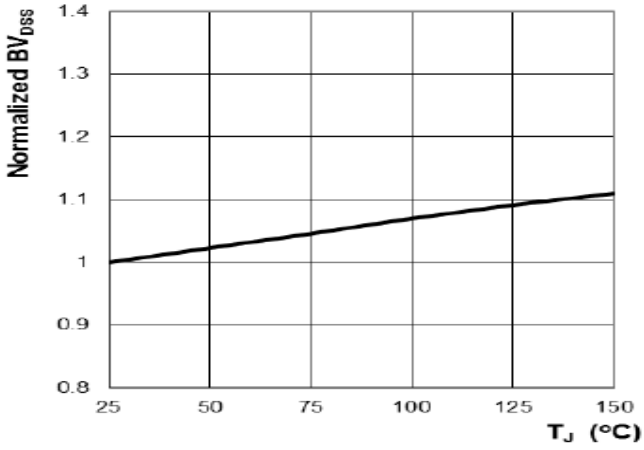



Figure 4: Normalized $BV_{DSS}$ vs. $T_J$

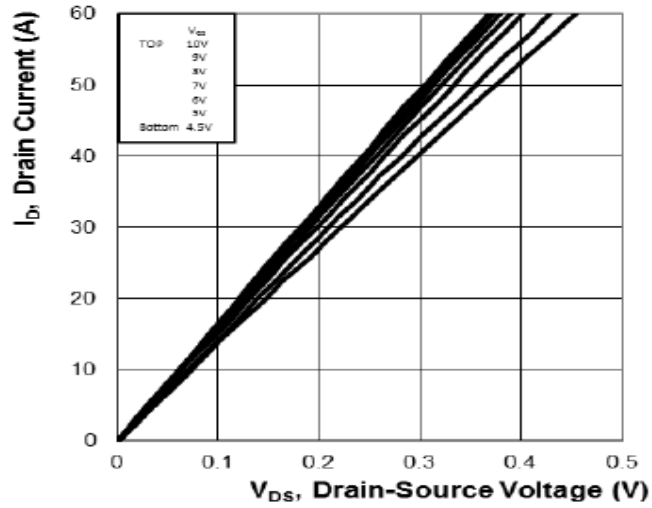



Figure 5: On-Region Characteristics

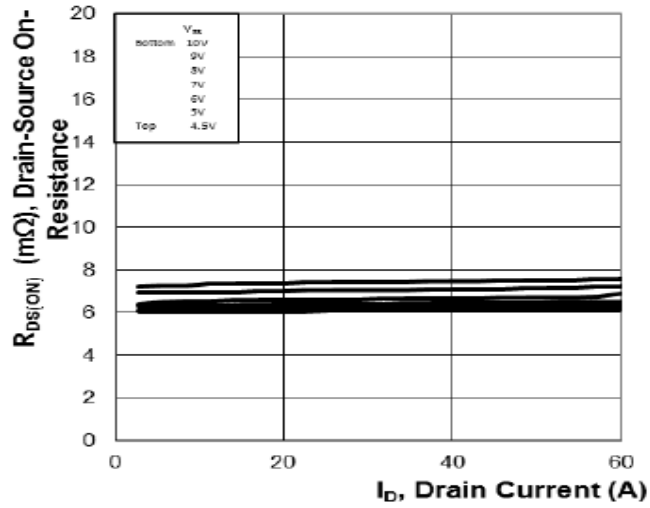



Figure 6: Typ. $R_{DS}$ Variation vs. $I_D$ and $V_{GS}$

## TYPICAL CHARACTERISTICS

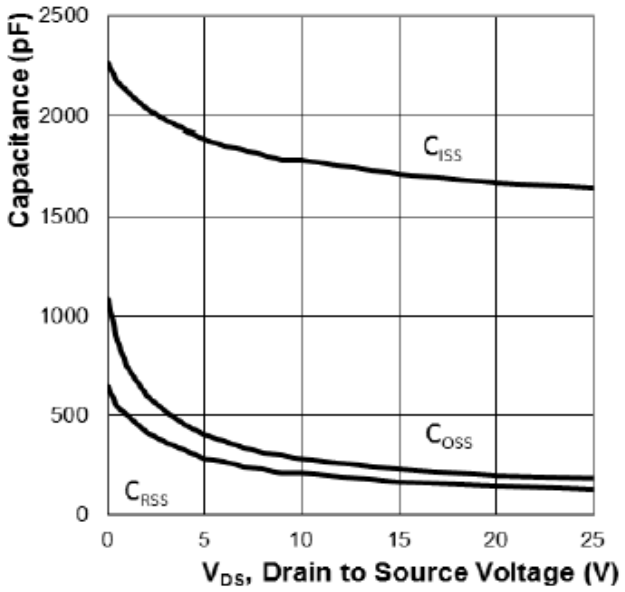



Figure 7: Typ. Capacitance Characteristics

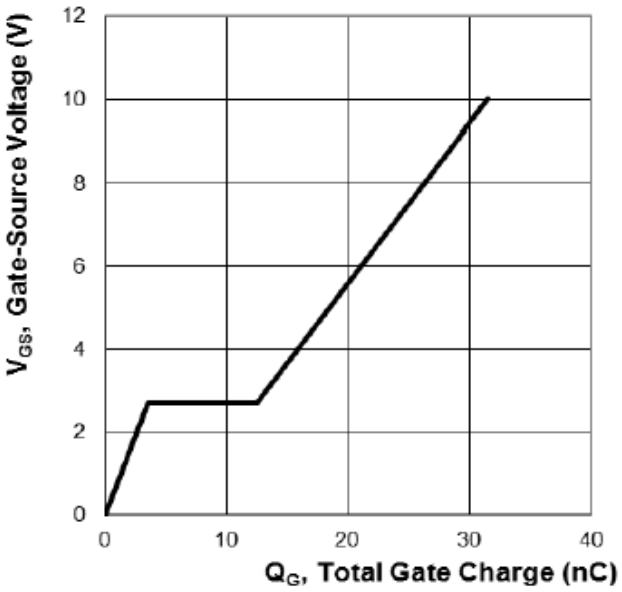



Figure 8: Typ. Gate Charge Characteristics

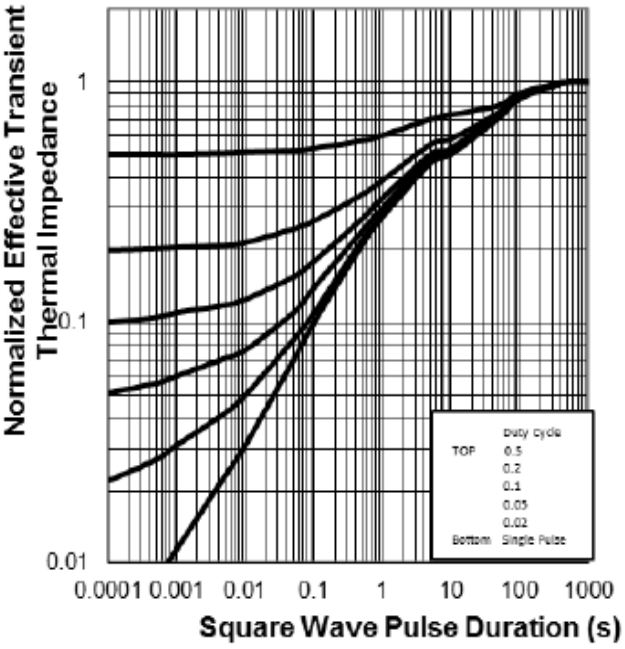



Figure 9: Normalized Thermal Transient Impedance, Junction-to-Case

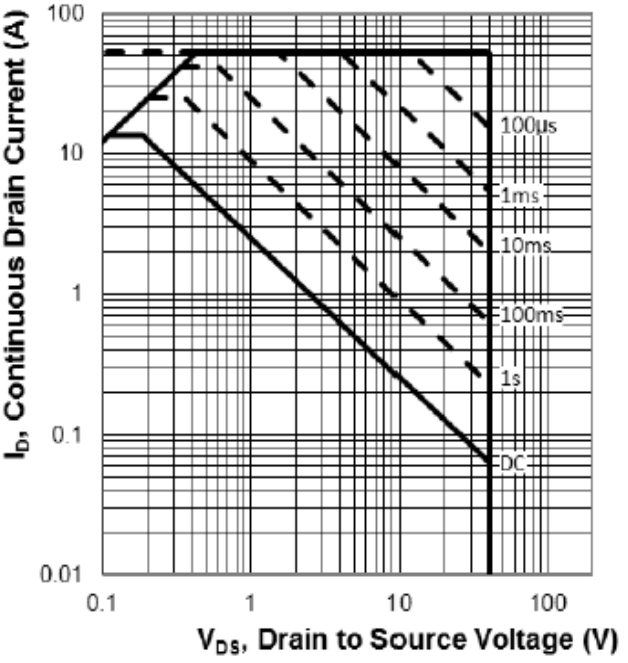
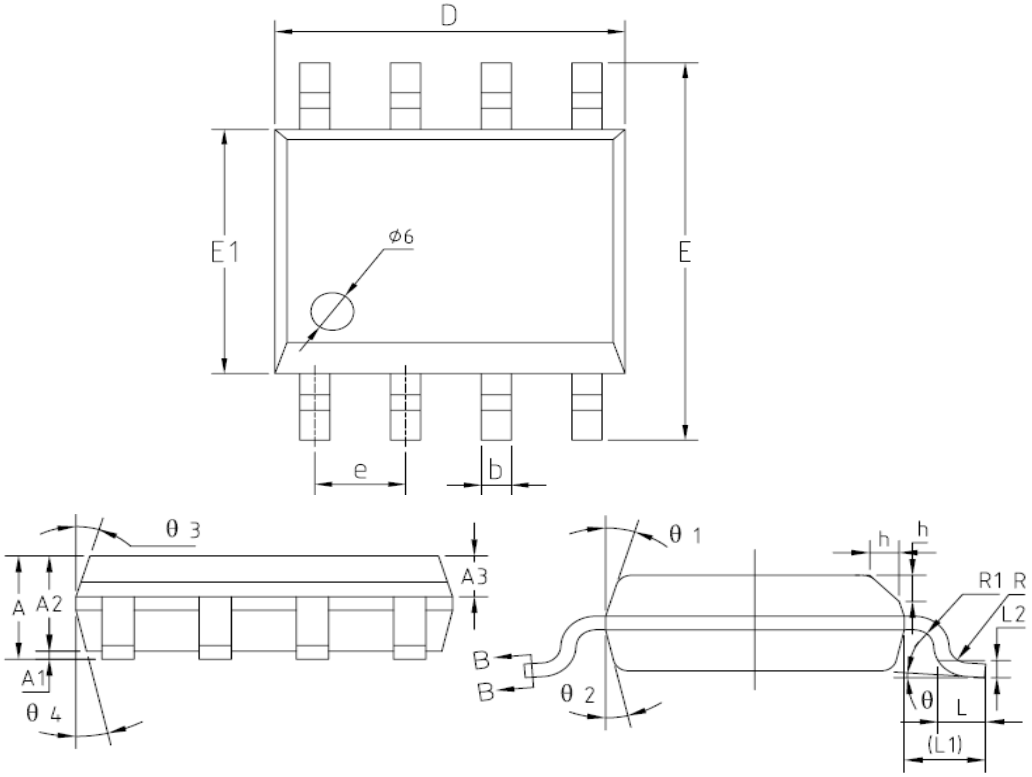



Figure 10: Maximum Safe Operation Area

**SOP- 8 PACKAGE OUTLINE**




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.35 | -- | 1.75 |
| A1 | 0.10 | -- | 0.25 |
| A2 | 1.25 | 1.40 | 1.65 |
| A3 | 0.50 | 0.60 | 0.70 |
| b | 0.33 | - | 0.51 |
| c | 0.17 | -- | 0.25 |
| D | 4.80 | 4.93 | 5.05 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.17 | 1.27 | 1.37 |
| L | 0.45 | 0.60 | 0.80 |
| L1 | 1.04 REF | | |
| L2 | 0.25BSC | | |
| R | 0.07 | -- | -- |
| R1 | 0.07 | -- | 0.20 |
| h | 0.25 | -- | 0.50 |
| θ | 0° | -- | 8° |
| θ 1 | 15° | 17° | 19° |
| θ 2 | 11° | 13° | 15° |
| θ 3 | 15° | 17° | 19° |
| θ 4 | 11° | 13° | 15° |

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