



SPN4844 N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4844 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching .

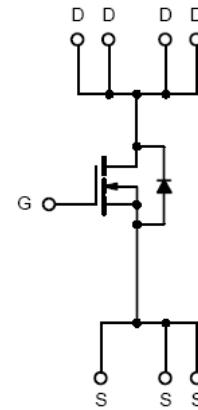
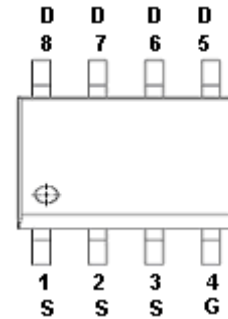
FEATURES

- ◆ 45V/15A, $R_{DS(ON)}=9.5m\Omega@V_{GS}=10V$
- ◆ 45V/8A, $R_{DS(ON)}=14m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

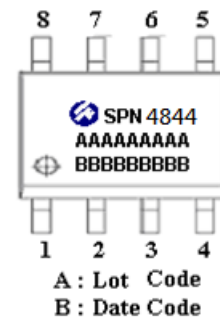
APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- Charger Adapter
- LED Lighting

PIN CONFIGURATION(SOP-8)



PART MARKING





SPN4844

N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

| Pin | Symbol | Description |
|-----|--------|-------------|
| 1 | S | Source |
| 2 | S | Source |
| 3 | S | Source |
| 4 | G | Gate |
| 5 | D | Drain |
| 6 | D | Drain |
| 7 | D | Drain |
| 8 | D | Drain |

ORDERING INFORMATION

| Part Number | Package | Part Marking |
|--------------|---------|--------------|
| SPN4844S8RGB | SOP-8 | SPN4844 |

※ SPN4844S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

| Parameter | Symbol | Typical | Unit | |
|--|------------------|-----------------------|------|---|
| Drain-Source Voltage | V _{DSS} | 45 | V | |
| Gate –Source Voltage | V _{GSS} | ±20 | V | |
| Continuous Drain Current | I _D | T _C =25°C | 13.5 | A |
| | | T _C =100°C | 8.5 | |
| Pulsed Drain Current | I _{DM} | 50 | A | |
| Single Pulse Avalanche Energy | E _{AS} | 20 | mJ | |
| Power Dissipation | P _D | 3.1 | W | |
| Operating Junction Temperature | T _J | -55/150 | °C | |
| Storage Temperature Range | T _{STG} | -55/150 | °C | |
| Thermal Resistance-Junction to Ambient | R _{θJA} | 75 | °C/W | |



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

| Parameter | Symbol | Conditions | Min. | Typ | Max. | Unit |
|---------------------------------|---------------|---|------|------|-----------|------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}=0V, I_D=250\mu A$ | 45 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=250\mu A$ | 1.0 | 1.55 | 2.2 | |
| Gate Leakage Current | I_{GSS} | $V_{DS}=0V, V_{GS}=\pm 20V$ | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=45V, V_{GS}=0V, T_J=25^\circ C$ | | | 1 | uA |
| | | $V_{DS}=45V, V_{GS}=0V, T_J=100^\circ C$ | | | 100 | |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}=10V, I_D=15A$ | | | 9.5 | mΩ |
| | | $V_{GS}=4.5V, I_D=8A$ | | | 14 | |
| Forward Transconductance | g_{fs} | $V_{DS}=5V, I_D=10A$ | | 8 | | S |
| Diode Forward Voltage | V_{SD} | $I_S=20A, V_{GS}=0V$ | | 0.9 | 1.2 | V |
| Dynamic | | | | | | |
| Total Gate Charge (10V) | Q_g | $V_{DS}=20V, V_{GS}=10V$ $I_D=10A$ | | 14.5 | | nC |
| Total Gate Charge (4.5V) | Q_g | | | 7 | | |
| Gate-Source Charge | Q_{gs} | | | 2 | | |
| Gate-Drain Charge | Q_{gd} | | | 2.5 | | |
| Input Capacitance | C_{iss} | $V_{DS}=20V, V_{GS}=0V$ $f=1MHz$ | | 942 | | pF |
| Output Capacitance | C_{oss} | | | 309 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 29 | | |
| Turn-On Time | $t_{d(on)}$ | $V_{DD}=20V, I_D=10A, V_{GS}=10V$ $R_G=10\Omega$ | | 6 | | nS |
| | t_r | | | 5 | | |
| Turn-Off Time | $t_{d(off)}$ | | | 21 | | |
| | t_f | | | 5 | | |
| Gate resistance | R_g | $V_{GS}=0V, V_{DS}=0V, f=1MHz$ | | 1.5 | | Ω |



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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

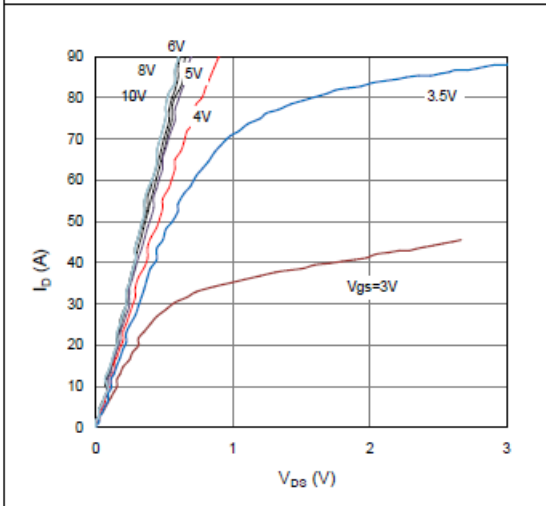


Figure 2. On-Resistance vs. Gate-Source Voltage

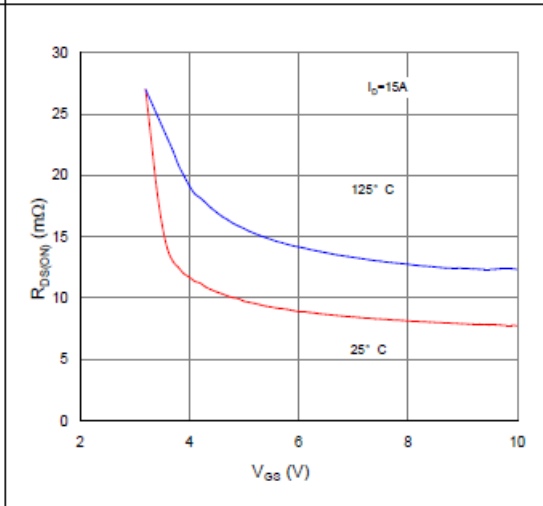


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

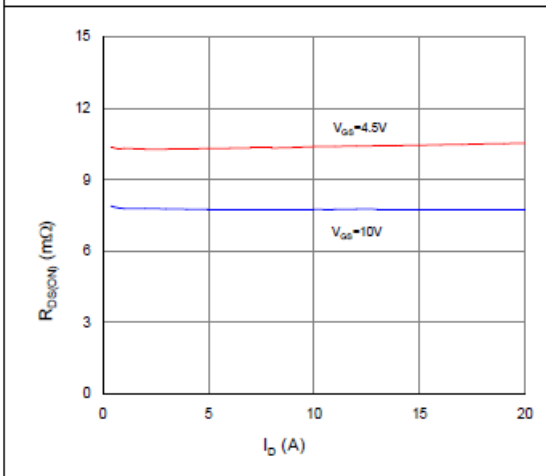


Figure 4. Normalized On-Resistance vs. Junction Temperature

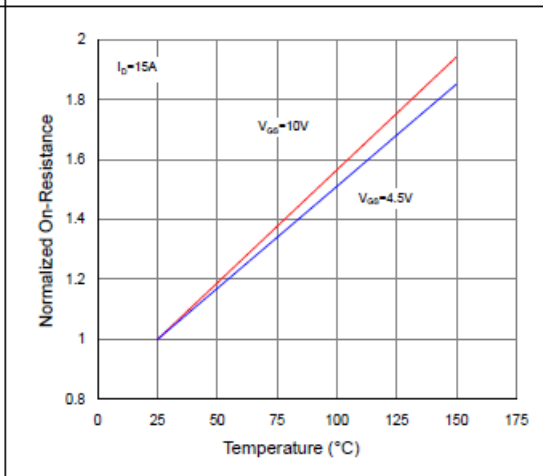


Figure 5. Typical Transfer Characteristics

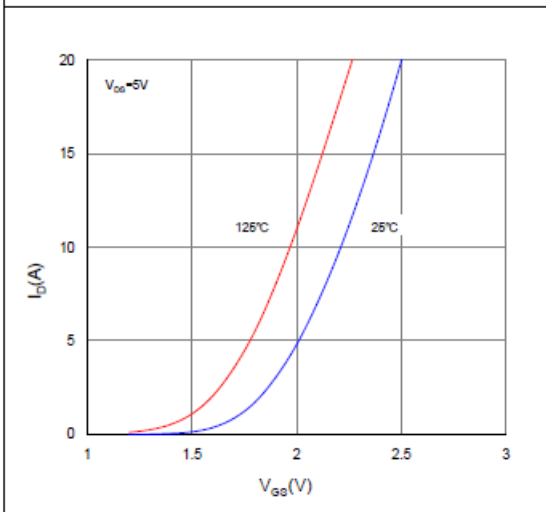
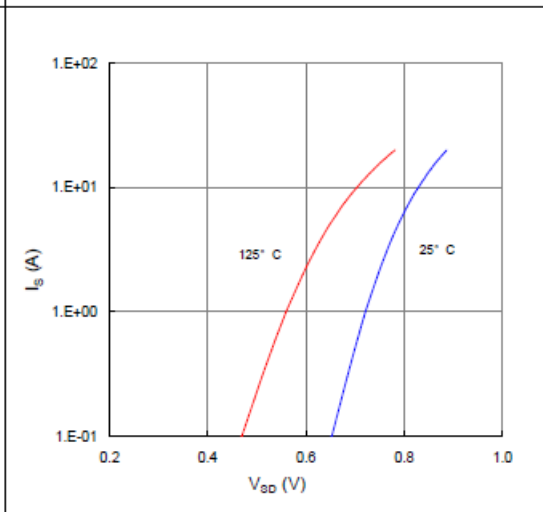


Figure 6. Typical Source-Drain Diode Forward Voltage





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TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

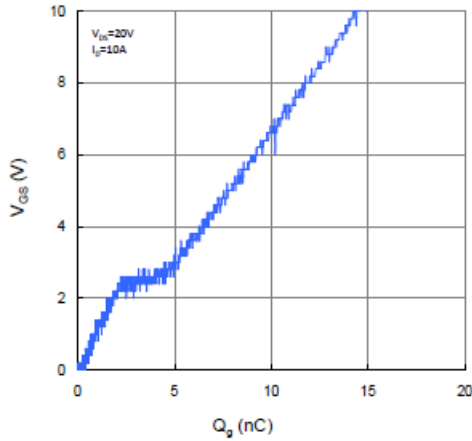


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

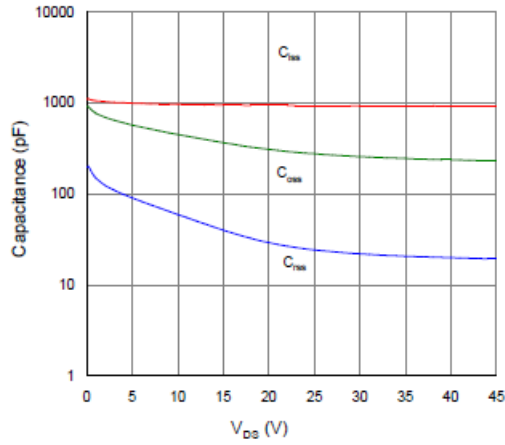


Figure 9. Maximum Safe Operating Area

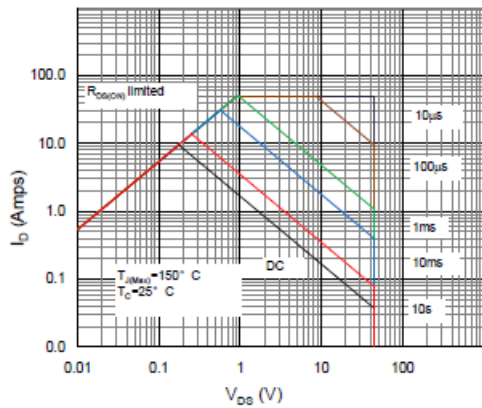


Figure 10. Maximum Drain Current vs. Case Temperature

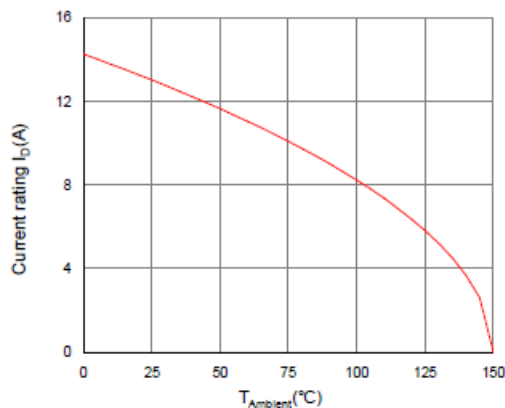
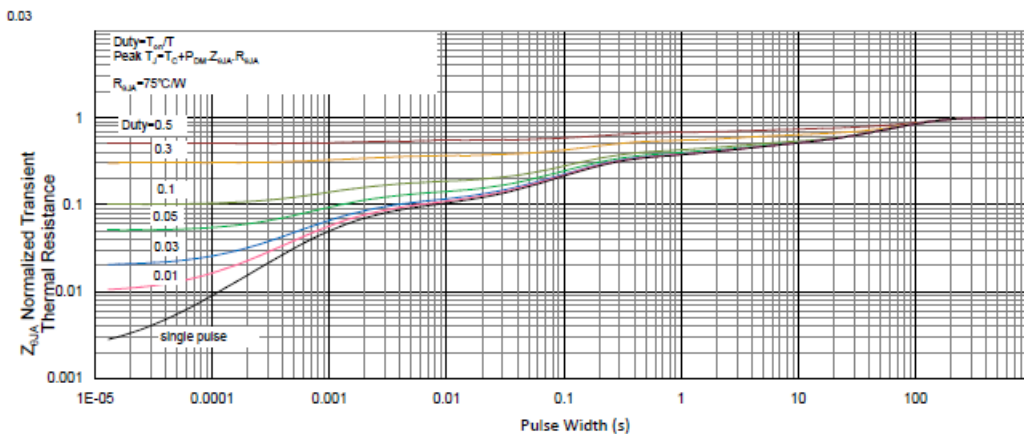


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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