



SPN4848

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4848 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching .

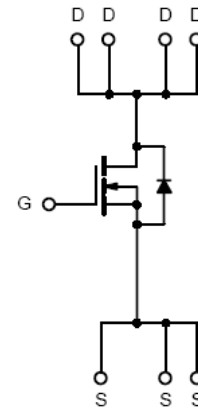
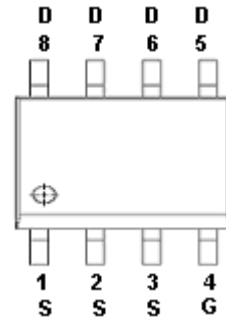
FEATURES

- ◆ 40V/7A, $R_{DS(ON)}=17m\Omega@V_{GS}=10V$
- ◆ 40V/6A, $R_{DS(ON)}=22m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- Charger Adapter
- LED Lighting

PIN CONFIGURATION(SOP-8)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4848S8RGB	SOP-8	SPN4848

※ SPN4848S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	40	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current	I _D	T _C =25°C	8.4	A
		T _C =70°C	6.7	
Pulsed Drain Current	I _{DM}	50	A	
Power Dissipation	P _D	1.9	W	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	65	°C/W	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=32V, V_{GS}=0V, T_J=25^\circ C$			1	uA
		$V_{DS}=32V, V_{GS}=0V, T_J=55^\circ C$			5	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=7A$			17	mΩ
		$V_{GS}=4.5V, I_D=6A$			22	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=7A$		32		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1.0	V
Dynamic						
Total Gate Charge (4.5V)	Q_g	$V_{DS}=32V, V_{GS}=4.5V$ $I_D=7A$		9.8		nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			3.9		
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		1013		pF
Output Capacitance	C_{oss}			107		
Reverse Transfer Capacitance	C_{rss}			76		
Turn-On Time	$t_{d(on)}$	$V_{DD}=20V, I_D=7A, V_{GS}=10V$ $R_G=3.3\Omega$		2.8		nS
	t_r			40.4		
Turn-Off Time	$t_{d(off)}$			22.8		
	t_f			6.4		
Gate resistance	R_g	$V_{GS}=0V, V_{DS}=0V, f=1MHz$		2.1		Ω



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TYPICAL CHARACTERISTICS

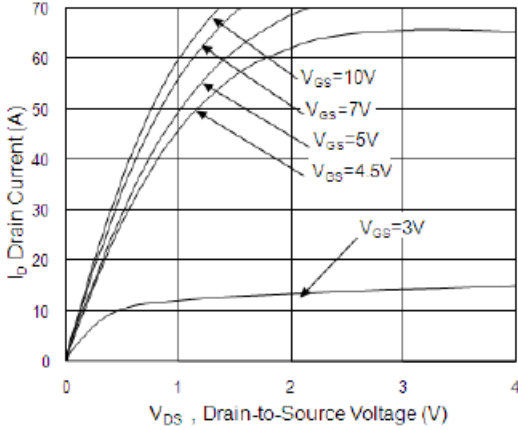


Fig.1 Typical Output Characteristics

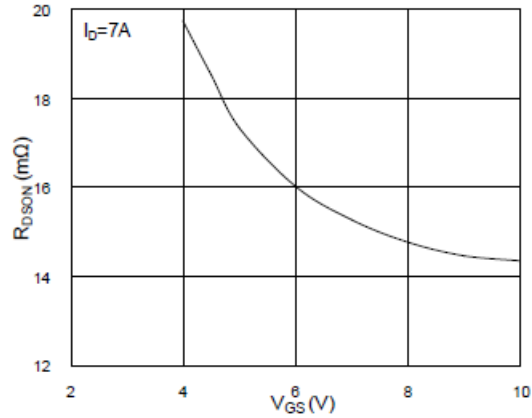


Fig.2 On-Resistance vs. G-S Voltage

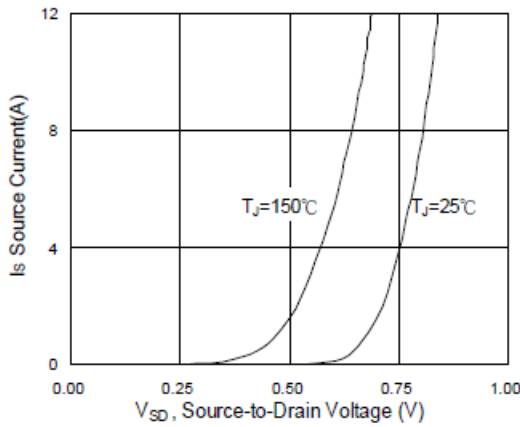


Fig.3 Forward Characteristics of Reverse

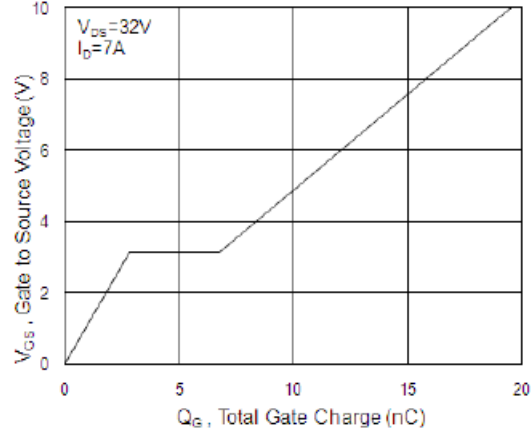


Fig.4 Gate-Charge Characteristics

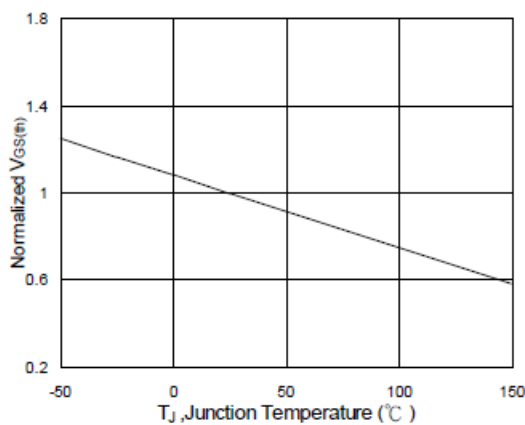


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

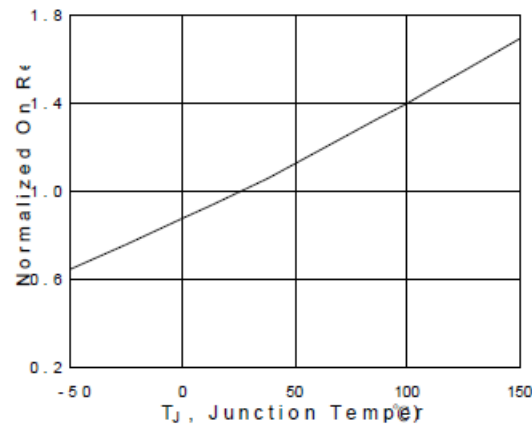


Fig.6 Normalized $R_{DS(on)}$ vs. T_J



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TYPICAL CHARACTERISTICS

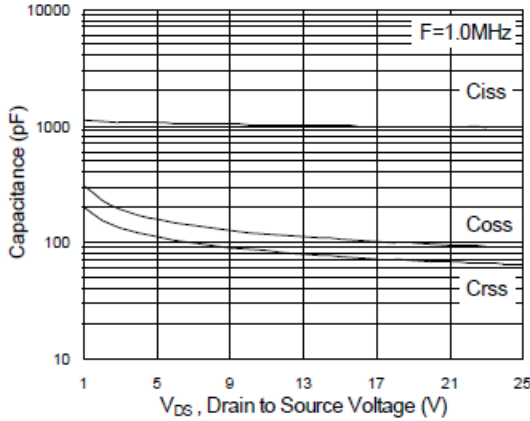


Fig.7 Capacitance

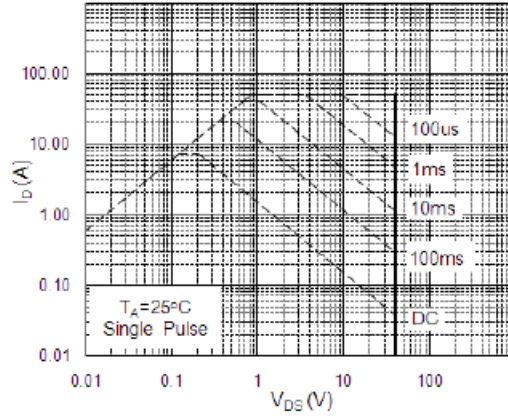


Fig.8 Safe Operating Area

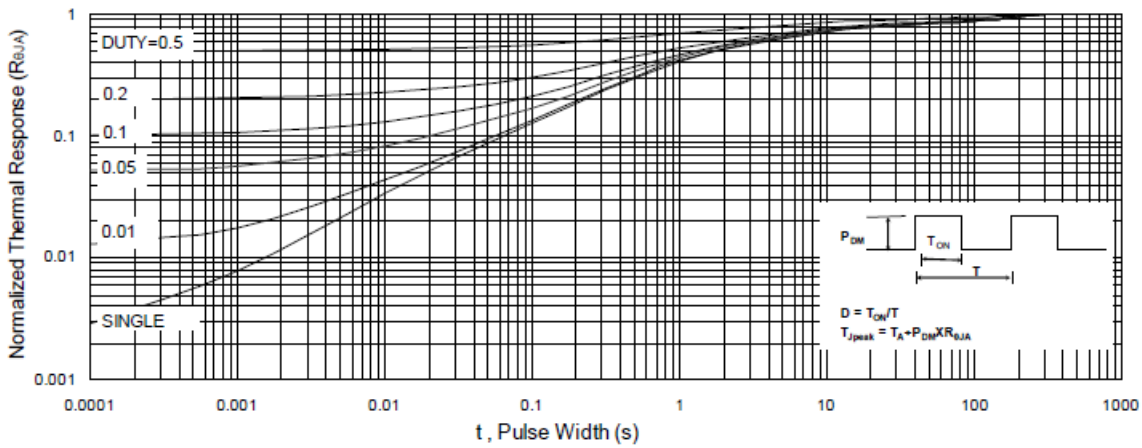


Fig.9 Normalized Maximum Transient Thermal Impedance

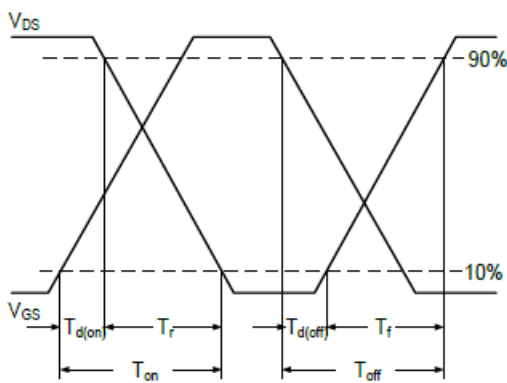


Fig.10 Switching Time Waveform

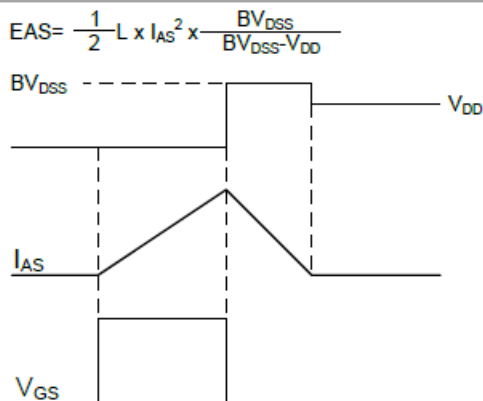


Fig.11 Unclamped Inductive Switching Waveform



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