



# SPN4850 N-Channel Enhancement Mode MOSFET

## DESCRIPTION

The SPN4850 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

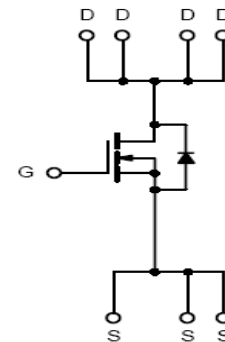
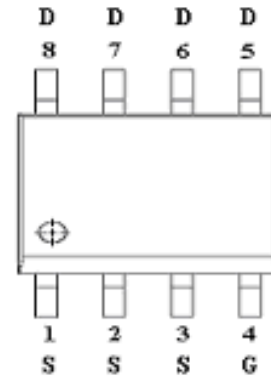
## FEATURES

- ◆ 65V/7.6A, $R_{DS(ON)}=35m\Omega@V_{GS}=10V$
- ◆ 65V/7.2A, $R_{DS(ON)}=40m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

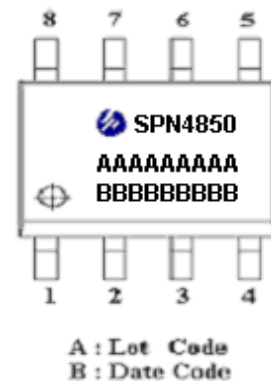
## APPLICATIONS

- DC/DC Converter
- Load Switch

## PIN CONFIGURATION(SOP-8)



## PART MARKING





# SPN4850

## N-Channel Enhancement Mode MOSFET

### PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4850S8RGB	SOP-8	SPN4850

※ SPN4850S8RGB : 13" Tape Reel ; Pb – Free ; Halogen -Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	65	V
Gate –Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C	7.6
		T <sub>A</sub> =70°C	6.8
Pulsed Drain Current	I <sub>DM</sub>	40	A
Avalanche Current	I <sub>AS</sub>	15	A
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C	2.5
		T <sub>A</sub> =70°C	1.6
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	80	°C/W



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

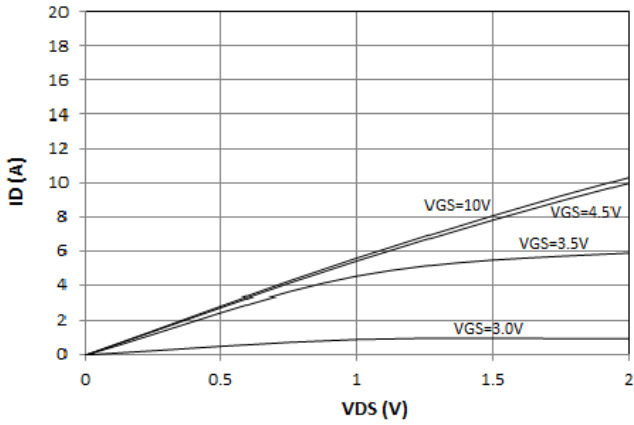
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	65			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=48V, V_{GS}=0V$			1	uA
		$V_{DS}=48V, V_{GS}=0V$ $T_J=55^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	25			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=7.6A$		23	35	mΩ
		$V_{GS}=4.5V, I_D=7.2A$		27	40	
Forward Transconductance	$g_{fs}$	$V_{DS}=15V, I_D=6.2A$		25		S
Diode Forward Voltage	$V_{SD}$	$I_S=7.6A, V_{GS}=0V$		0.8	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=30V, V_{GS}=10V$ $I_D=6A$		25	30	nC
Gate-Source Charge	$Q_{gs}$			4.2		
Gate-Drain Charge	$Q_{gd}$			5.3		
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V$ $f=1MHz$		1476		pF
Output Capacitance	$C_{oss}$			76		
Reverse Transfer Capacitance	$C_{rss}$			60		
Turn-On Time	$t_{d(on)}$	$V_{DD}=30V, R_L=30\Omega$ $I_D=1.0A, V_{GEN}=10V$ $R_G=6\Omega$		10	20	nS
	$t_r$			10	20	
Turn-Off Time	$t_{d(off)}$			25	50	
	$t_f$			12	25	



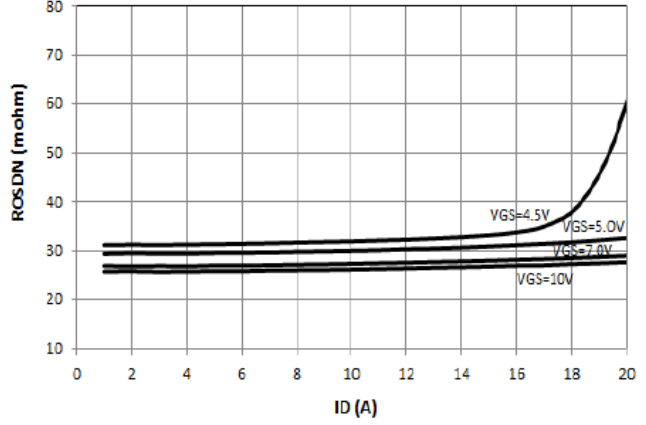
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## TYPICAL CHARACTERISTICS

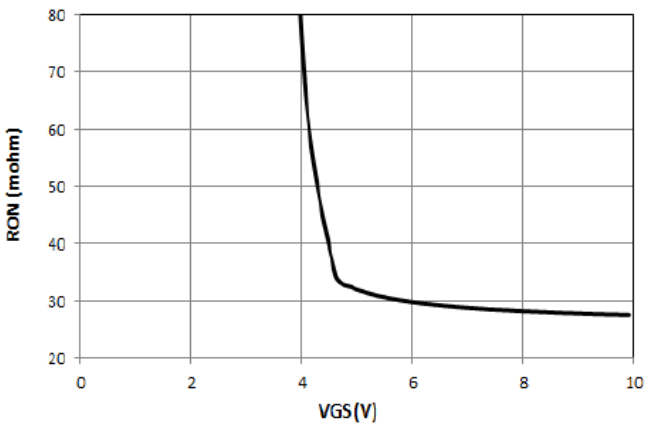
TYPICAL OUTPUT CHARACTERISTICS



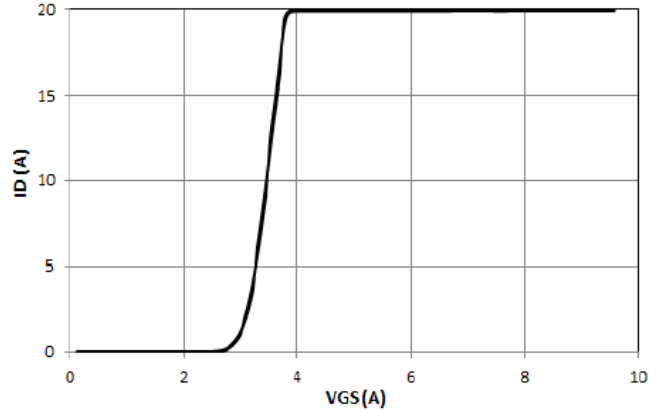
ON-RESISTANCE VS. DRAIN CURRENT AND GATE VOLTAGE



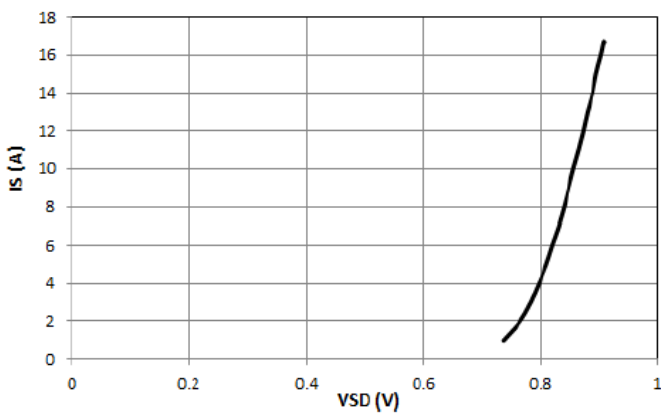
ON-RESISTANCE VS. GATE-SOURCE VOLTAGE



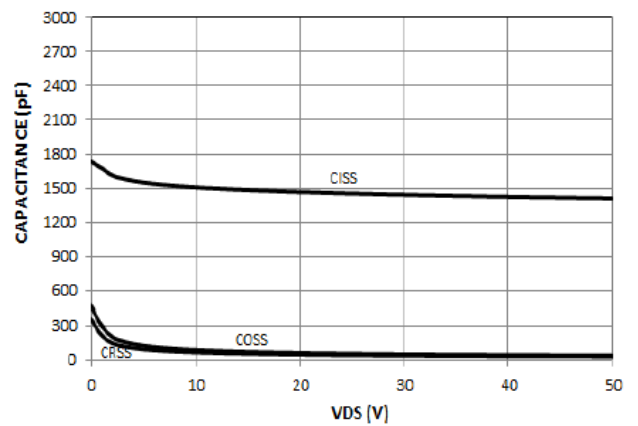
TYPICAL TRANSFER CHARACTERISTICS



TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE



TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE

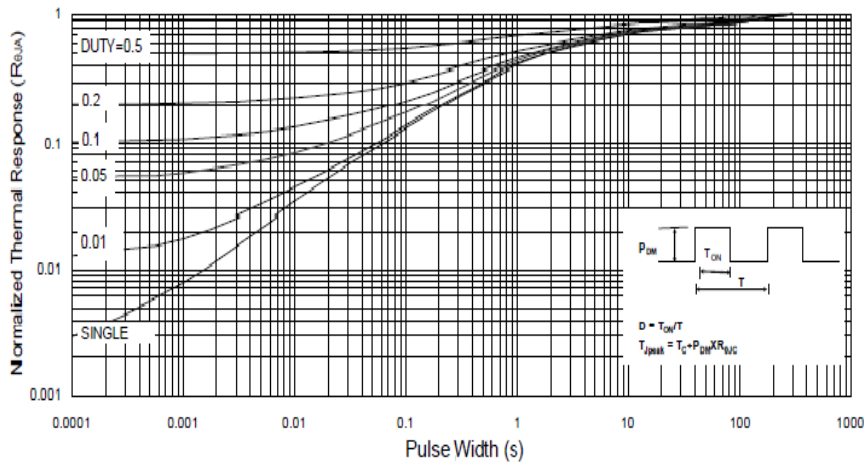




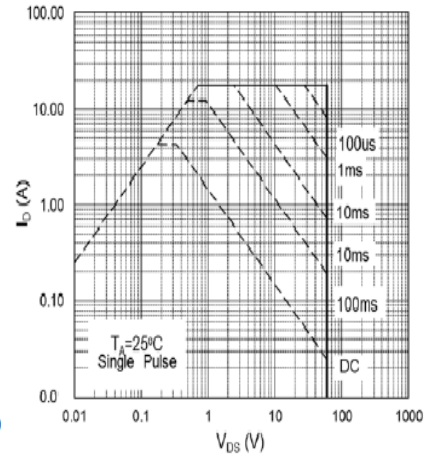
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## TYPICAL CHARACTERISTICS

Normalized Maximum Transient Thermal Impedance, Junction-to-Case



Maximum Safe Operating Area





# SPN4850

## N-Channel Enhancement Mode MOSFET

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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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