



SPN4852

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4852 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

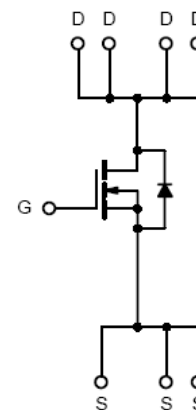
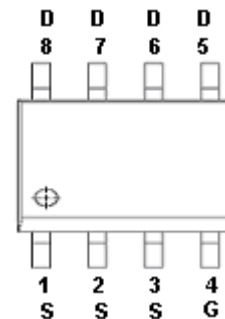
FEATURES

- ◆ 150V/4.1A, $R_{DS(ON)}=88m\Omega@V_{GS}=10V$
- ◆ 150V/2A, $R_{DS(ON)}=100m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

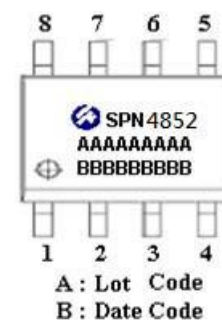
APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

PIN CONFIGURATION(SOP-8)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4852S8RGB	SOP-8	SPN4852

※ SPN4852S8RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	150	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	4.1	A
Pulsed Drain Current	I _{DM}	20	A
Avalanche Energy, Single Pulse (L=0.1mH , T _c =25°C)	E _{AS}	40	mJ
Power Dissipation	P _D	5.0	W
		2.5	
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case	R _{θJC}	25	°C/W
Thermal Resistance-Junction to Ambient (steady state)	R _{θJA}	50	



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ELECTRICAL CHARACTERISTICS

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Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	150			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2		2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=120V, V_{GS}=0V$ $T_J=25^\circ C$			1	uA
		$V_{DS}=120V, V_{GS}=0V$ $T_J=100^\circ C$			100	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4.1A$			88	mΩ
		$V_{GS}=4.5V, I_D=2A$			100	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=10A$		33		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1.0	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=75V, V_{GS}=4.5V,$ $I_D=10A$		25.1		nC
Gate-Source Charge	Q_{gs}			8.8		
Gate-Drain Charge	Q_{gd}			12.6		
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1MHz$		2280		pF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			83		
Turn-On Time	$t_{d(on)}$	$V_{DD}=75V,$ $I_D=10A, V_{GS}=10V$ $R_G=3.3\Omega$		13		nS
	t_r			8.2		
Turn-Off Time	$t_{d(off)}$			25		
	t_f			11		



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TYPICAL CHARACTERISTICS

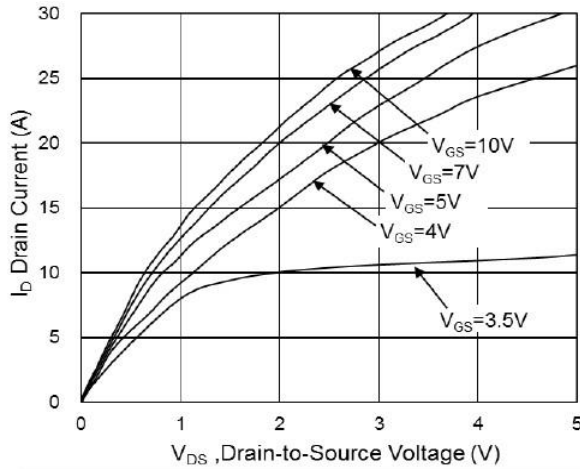


Fig.1 Typical Output Characteristics

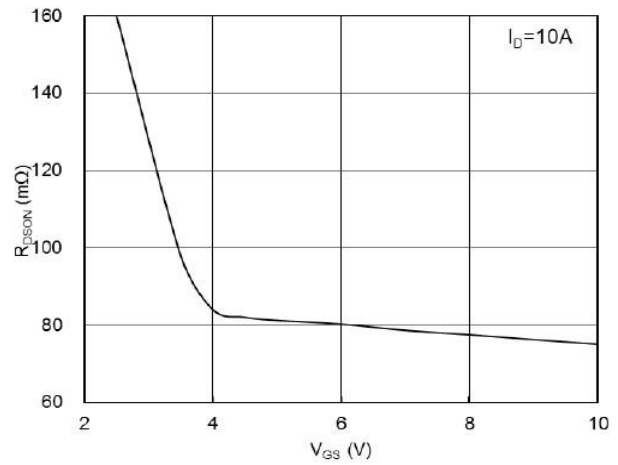


Fig.2 On-Resistance vs. Gate-Source Voltage

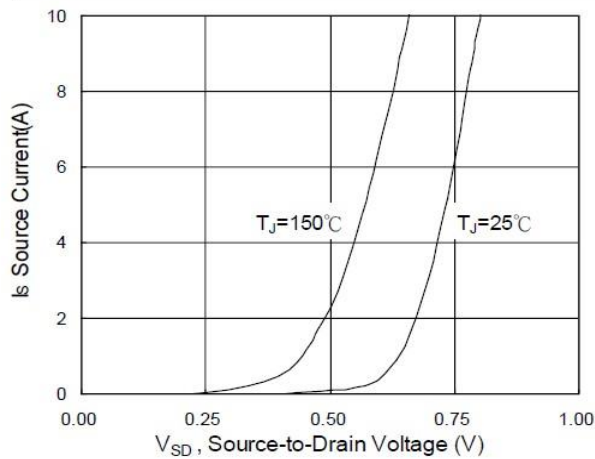


Fig.3 Forward Characteristics of Reverse

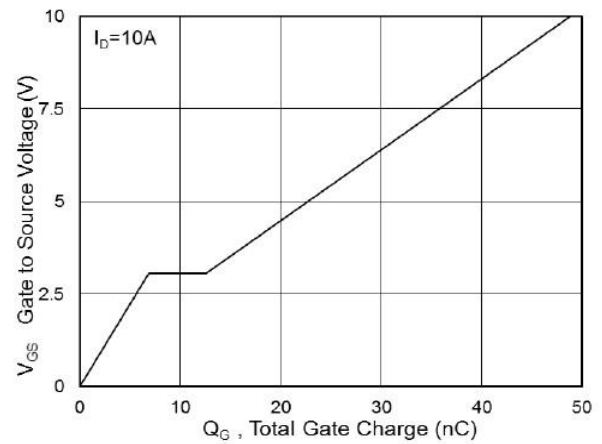


Fig.4 Gate-Charge Characteristics

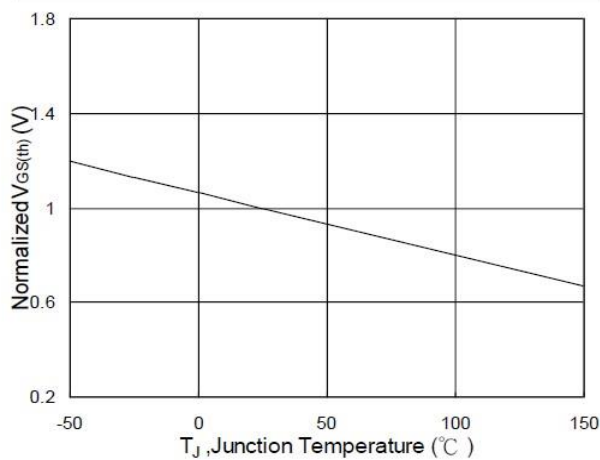


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

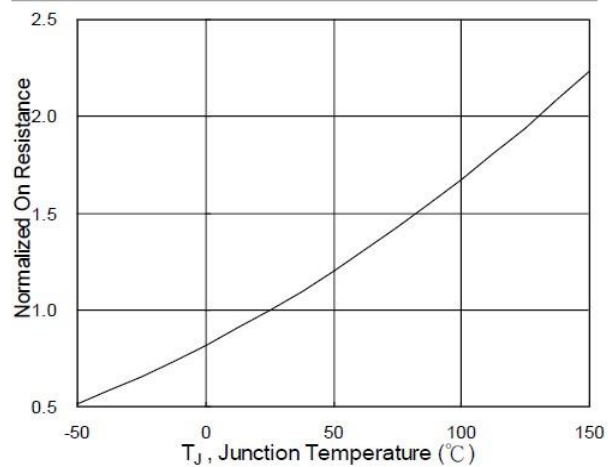


Fig.6 Normalized $R_{DS(on)}$ vs. T_J



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TYPICAL CHARACTERISTICS

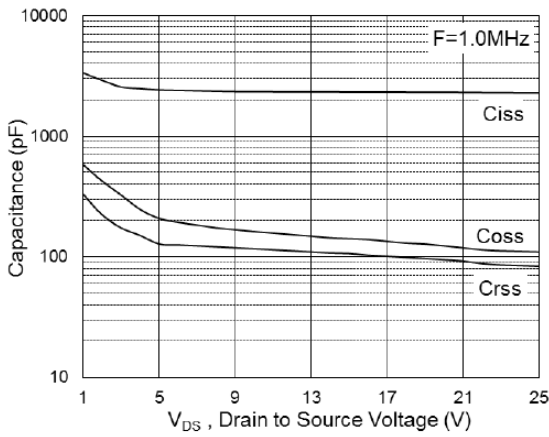


Fig.7 Capacitance

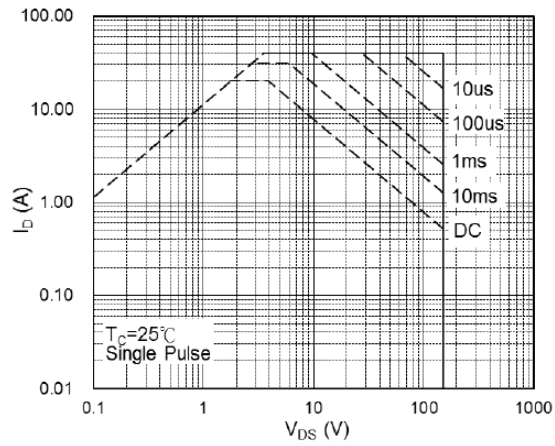


Fig.8 Safe Operating Area

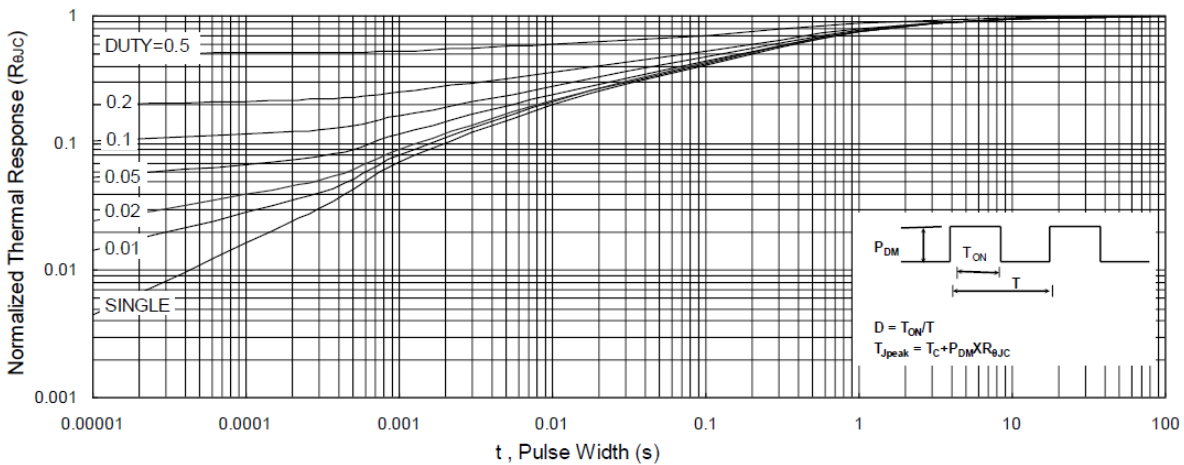


Fig.9 Normalized Maximum Transient Thermal Impedance

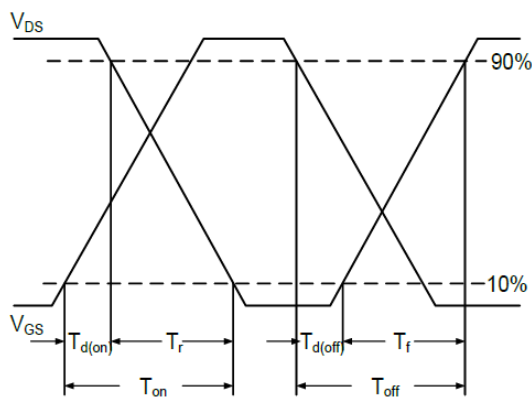


Fig.10 Switching Time Waveform

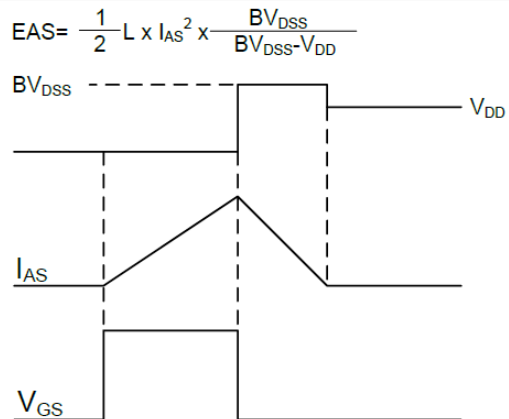


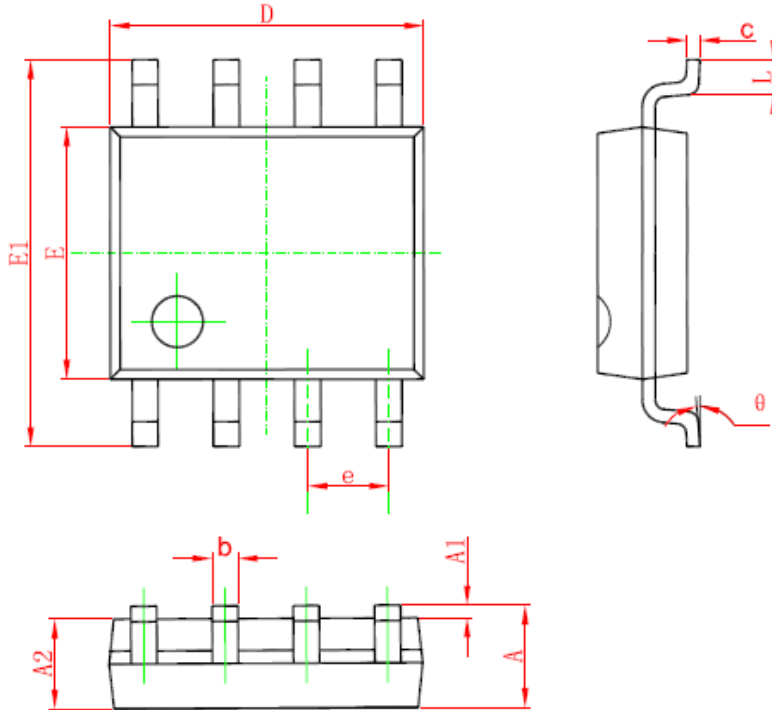
Fig.11 Unclamped Inductive Switching Waveform



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SOP-8 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



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