



# SPN4862

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN4862 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

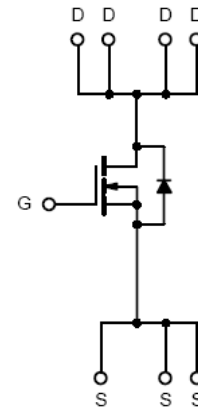
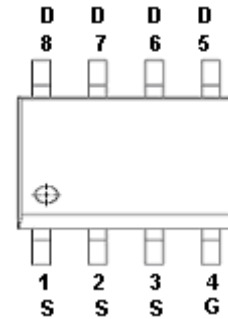
### FEATURES

- ◆ 60V/15A,  $R_{DS(ON)}=13m\Omega@V_{GS}=10V$
- ◆ 60V/10A,  $R_{DS(ON)}=17m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8P package design

### APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter

### PIN CONFIGURATION(SOP – 8P)



### PART MARKING





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### PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4862S8RGB	SOP-8P	SPN4862

※ SPN4862S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	60	V
Gate –Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	10
		TA=70°C	7
Pulsed Drain Current	I <sub>DM</sub>	60	A
Avalanche Current	I <sub>AS</sub>	38	A
Power Dissipation	P <sub>D</sub>	TA=25°C	2.5
		TA=70°C	1.6
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	80	°C/W



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=48V, V_{GS}=0V$			1	uA
		$V_{DS}=48V, V_{GS}=0V$ $T_J=55^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	60			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=15A$		11.5	13	mΩ
		$V_{GS}=4.5V, I_D=10A$		12	17	
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=15A$		47		S
Diode Forward Voltage	$V_{SD}$	$I_S=60A, V_{GS}=0V$			1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=48V, V_{GS}=4.5V$ $I_D=12A$		24		nC
Gate-Source Charge	$Q_{gs}$			6.9		
Gate-Drain Charge	$Q_{gd}$			10		
Input Capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		3200		pF
Output Capacitance	$C_{oss}$			210		
Reverse Transfer Capacitance	$C_{rss}$			145		
Turn-On Time	$t_{d(on)}$	$V_{DD}=30V,$ $I_D=2A, V_{GEN}=10V$ $R_G=3.3\Omega$		20		nS
	$t_r$			4		
Turn-Off Time	$t_{d(off)}$			84.5		
	$t_f$			6.5		



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## TYPICAL CHARACTERISTICS

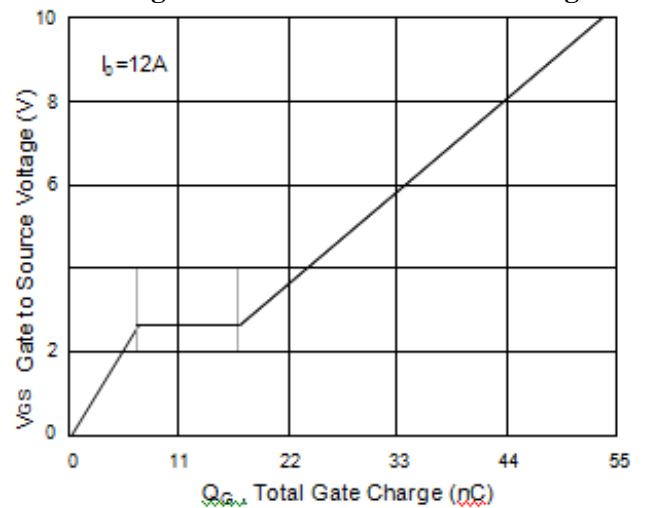
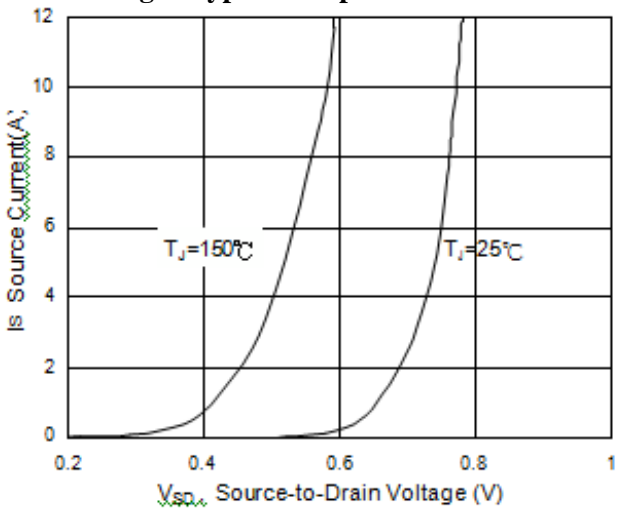
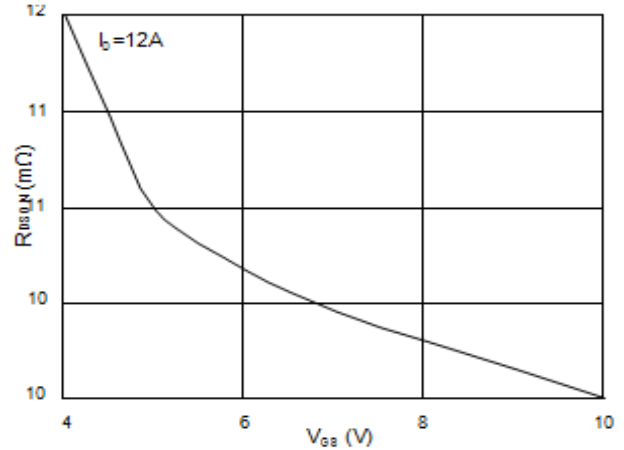
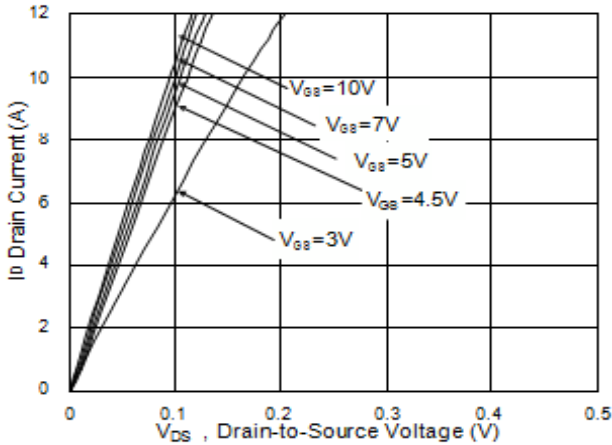
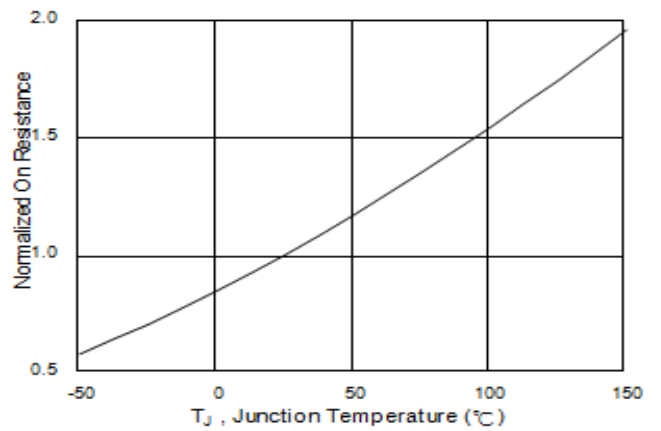
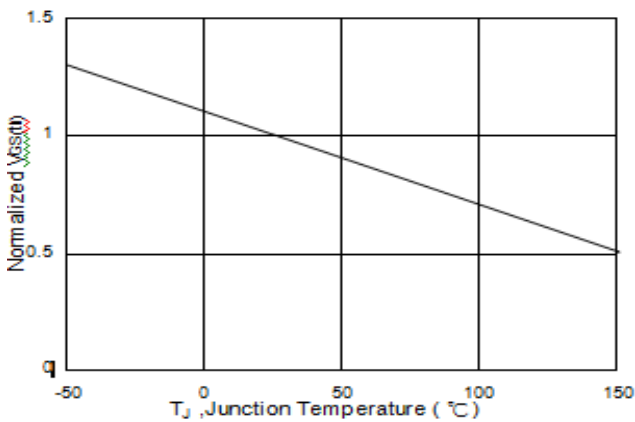


Fig. 3 Forward Characteristics  
Reverse Diodes

Fig. 4 Gate Charge Characteristics





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## TYPICAL CHARACTERISTICS

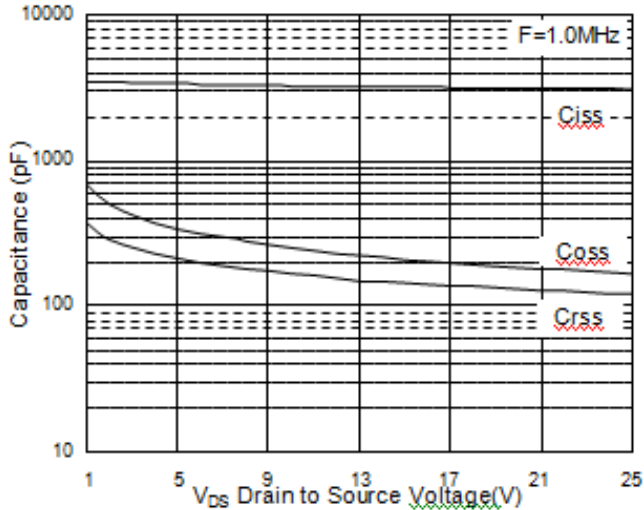


Fig. 7 Typical Capacitance Characteristics

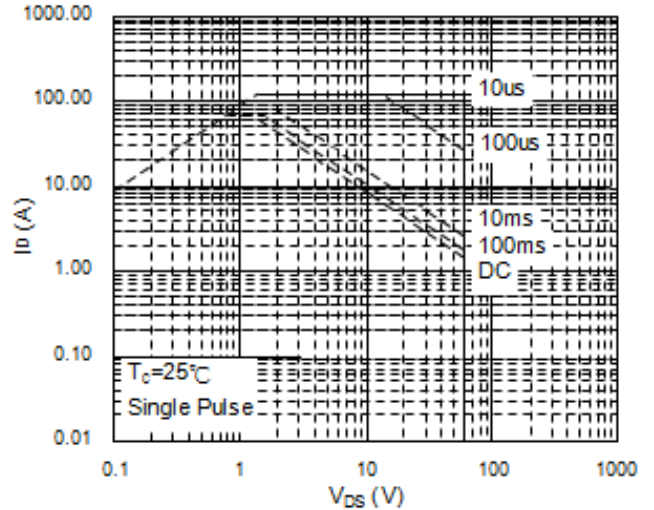


Fig. 8 Maximum Safe Operation Area

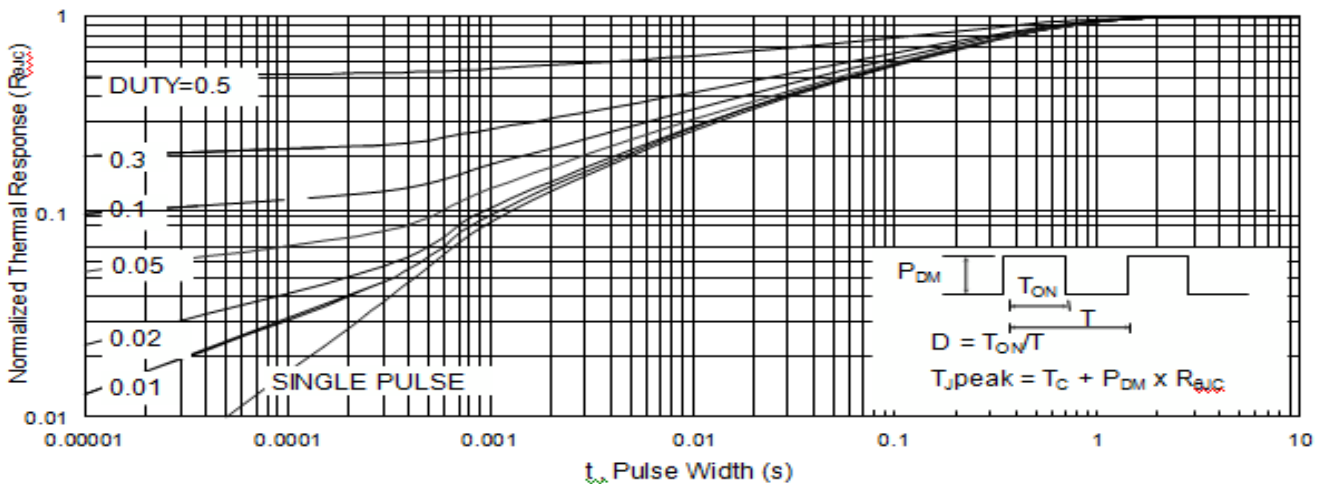


Fig. 9 Effective Transient Thermal Impedance

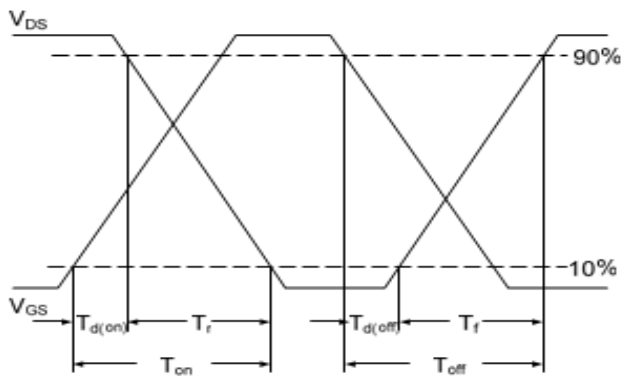


Fig. 10 Switching Time Waveform

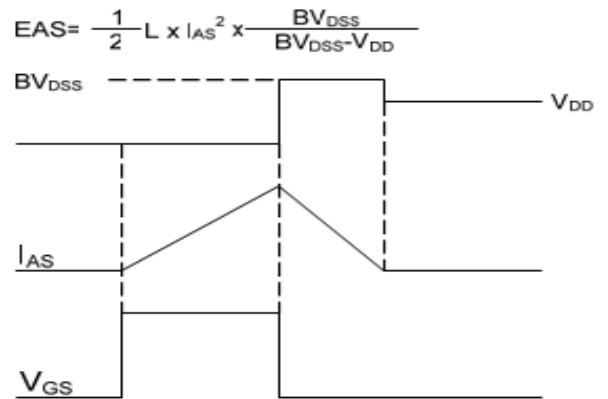


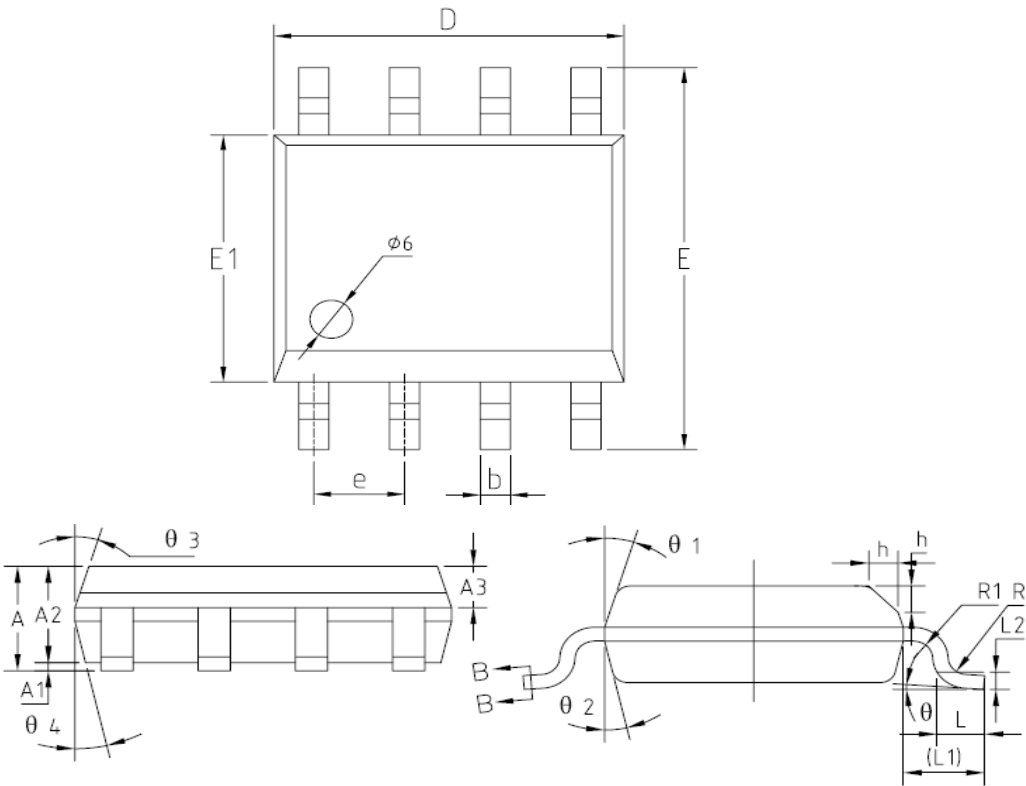
Fig. 11 Unclamped Inductive Waveform



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### SOP-8 PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	1.35	--	1.75
A1	0.10	--	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.33	-	0.51
c	0.17	--	0.25
D	4.80	4.93	5.05
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25BSC		
R	0.07	--	--
R1	0.07	--	0.20
h	0.25	--	0.50
$\theta$	0°	--	8°
$\theta 1$	15°	17°	19°
$\theta 2$	11°	13°	15°
$\theta 3$	15°	17°	19°
$\theta 4$	11°	13°	15°



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