



SPN4866

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4866 is the N-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high efficiency and fast switching is required.

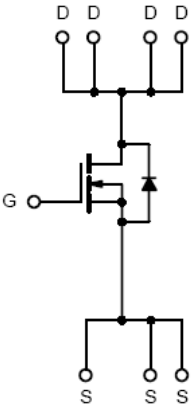
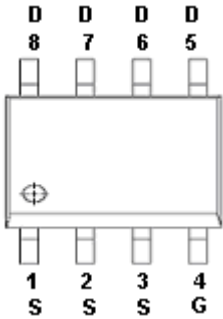
FEATURES

- ◆ 60V/6A, $R_{DS(ON)}=16m\Omega@V_{GS}=10V$
- ◆ 60V/6A, $R_{DS(ON)}=20m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

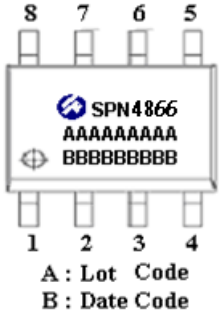
APPLICATIONS

- Motor Drive
- Power Tools
- LED Lighting
- Quick Charger

PIN CONFIGURATION (SOP-8)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4866S8RGB	SOP-8	SPN4866

※ SPN4866S8RGB : Tape Reel ; Pb – Free; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	60	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	T _C =25°C	6.5	A
		T _C =100°C	4.1	
Pulsed Drain Current	I _{DM}	26	A	
Avalanche Energy Single Pulse(L=0.1mH, T _C =25°C)	E _{AS}	36	mJ	
Power Dissipation	P _D	1.5	W	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	85	°C/W	
Thermal Resistance-Junction to Case	R _{θJC}	23	°C/W	



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ELECTRICAL CHARACTERISTICS

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Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1.3		3.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=48V, V_{GS}=0V,$ $T_J=25^\circ C$			1	uA
		$V_{DS}=48V, V_{GS}=0V,$ $T_J=150^\circ C$			100	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=6A$		13	16	m Ω
		$V_{GS}=4.5V, I_D=6A$		16	20	
Gate Resistance	R_G			1.3		Ω
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=3A$		15		S
Diode Forward Voltage	V_{SD}	$I_S=6A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	$Q_{g(10V)}$	$V_{DS}=48V, V_{GS}=10V,$ $I_D=6A$		29		nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			8		
Total Gate Charge	$Q_{g(4.5V)}$	$V_{DS}=48V, V_{GS}=4.5V$ $I_D=6A$		15		
Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $F=1MHz$		1400		pF
Output Capacitance	C_{oss}			137		
Reverse Transfer Capacitance	C_{rss}			95		
Turn-On Time	$t_{d(on)}$	$(V_{DD}=48V, I_D=6A,$ $V_{GEN}=10V, R_G=2.5\Omega)$		8.4		nS
	t_r			12.4		
Turn-Off Time	$t_{d(off)}$			26		
	t_f			4.4		



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TYPICAL CHARACTERISTICS

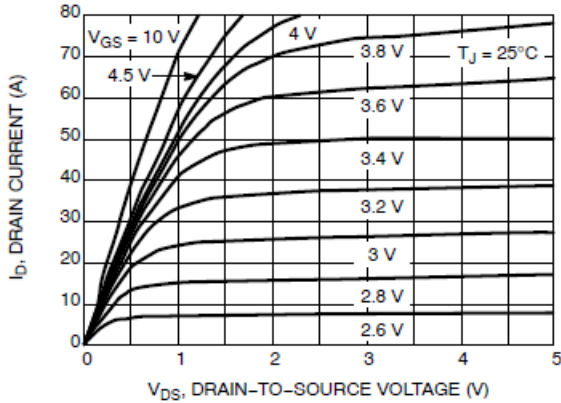


Figure 1. On-Region Characteristics

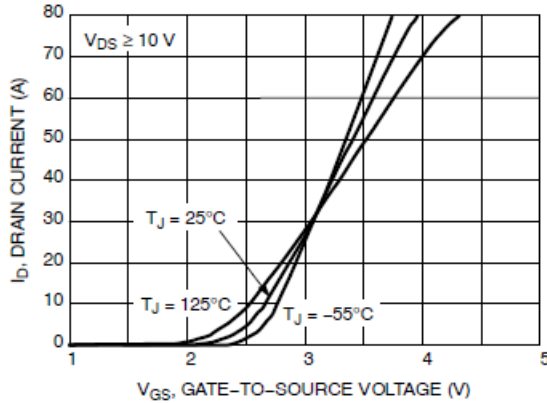


Figure 2. Transfer Characteristics

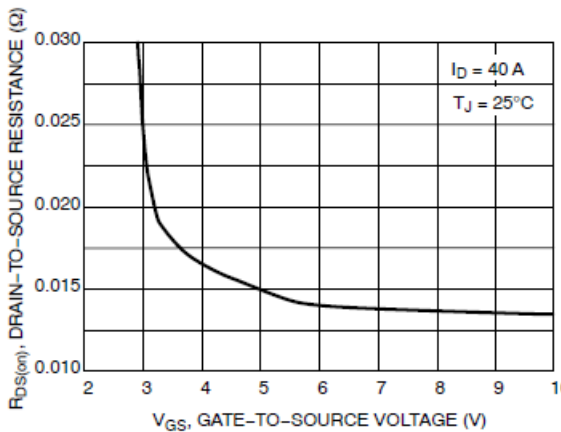


Figure 3. On-Resistance vs. Gate Voltage

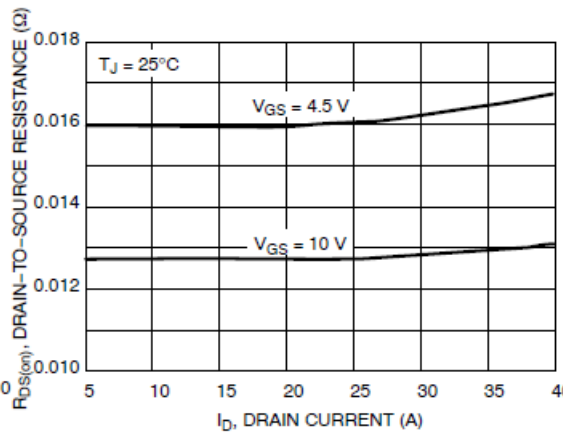


Figure 4. On-Resistance vs. Drain Current

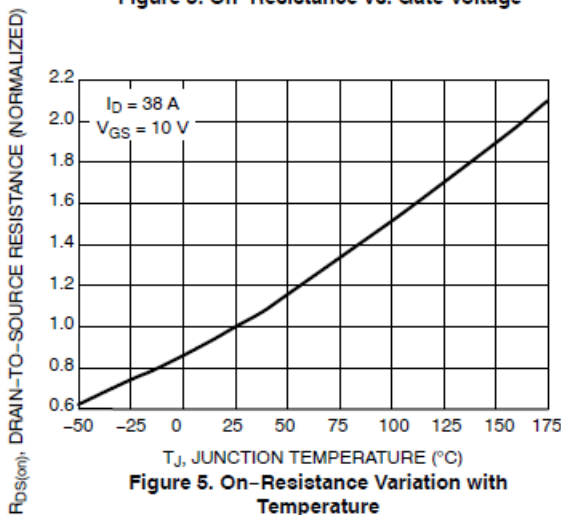


Figure 5. On-Resistance Variation with Temperature

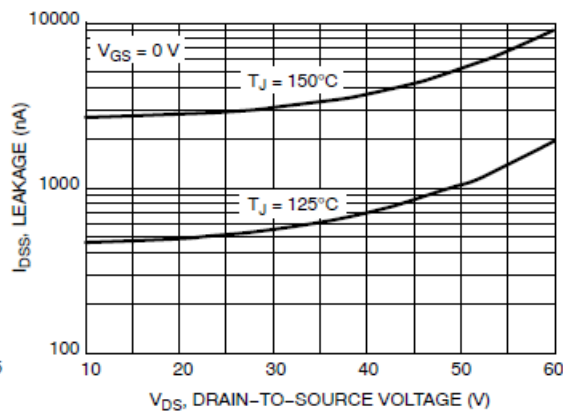


Figure 6. Drain-to-Source Leakage Current vs. Voltage



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TYPICAL CHARACTERISTICS

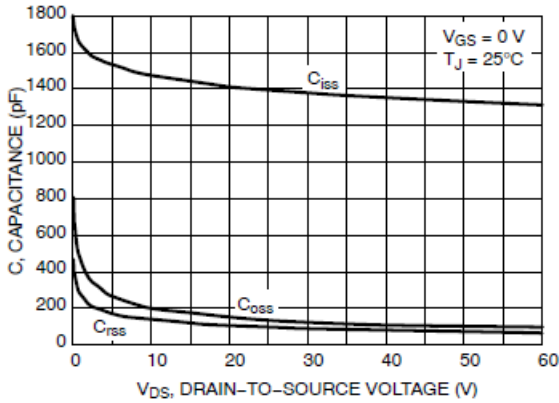


Figure 7. Capacitance Variation

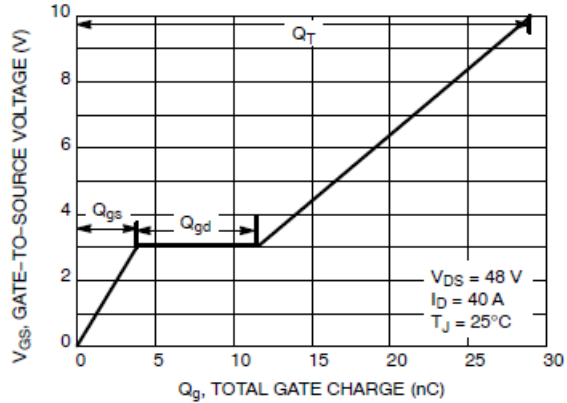


Figure 8. Gate-to-Source vs. Total Charge

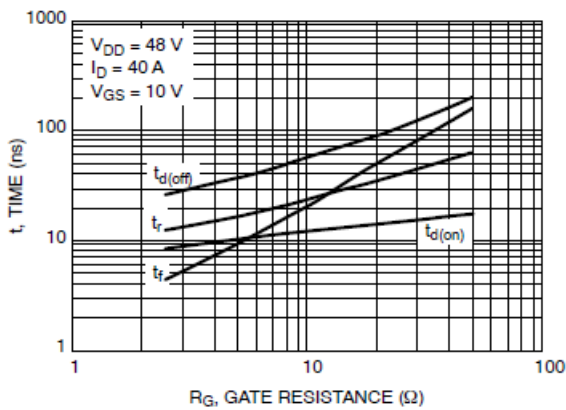


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

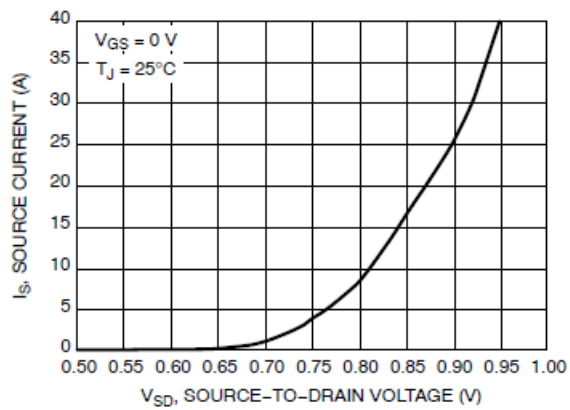


Figure 10. Diode Forward Voltage vs. Current

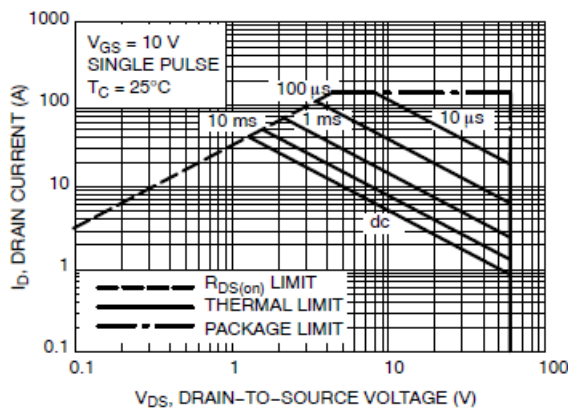


Figure 11. Maximum Rated Forward Biased Safe Operating Area



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