



SPN4946

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4946 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

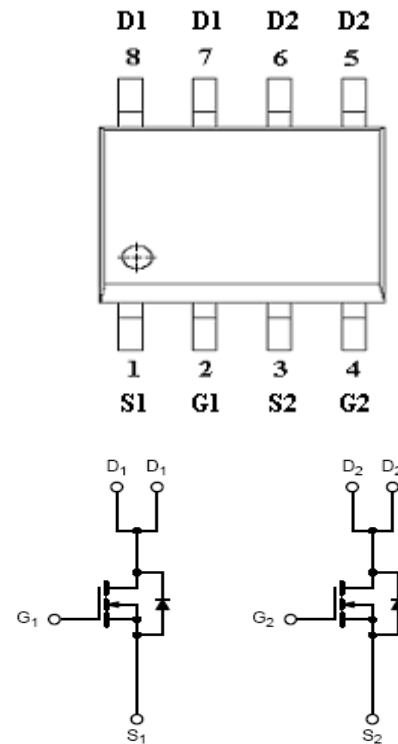
FEATURES

- ◆ 60V/12A, $R_{DS(ON)} = 45m\Omega @ V_{GS} = 10V$
- ◆ 60V/ 8A, $R_{DS(ON)} = 50m\Omega @ V_{GS} = 4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOP – 8P)



PART MARKING



A : Lot Code
B : Date Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4946S8RGB	SOP- 8P	SPN4946

※ SPN4946S8RGB: 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	60	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	T _A =25°C	7.0
		T _A =70°C	6.0
Pulsed Drain Current	I _{DM}	30	A
Avalanche Current	I _{AS}	11	A
Power Dissipation	P _D	T _A =25°C	2.5
		T _A =70°C	1.6
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	80	°C/W



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ELECTRICAL CHARACTERISTICS

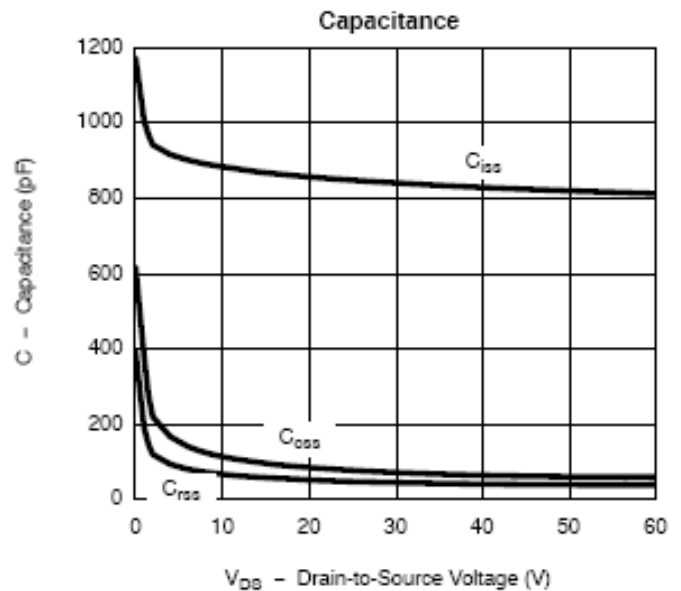
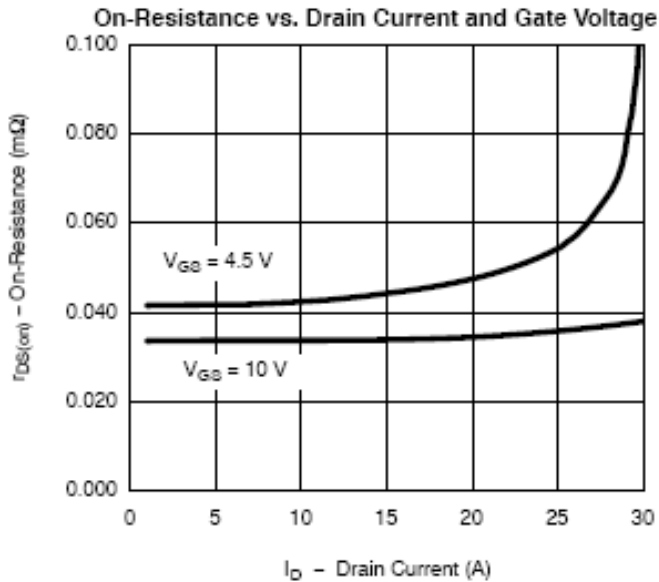
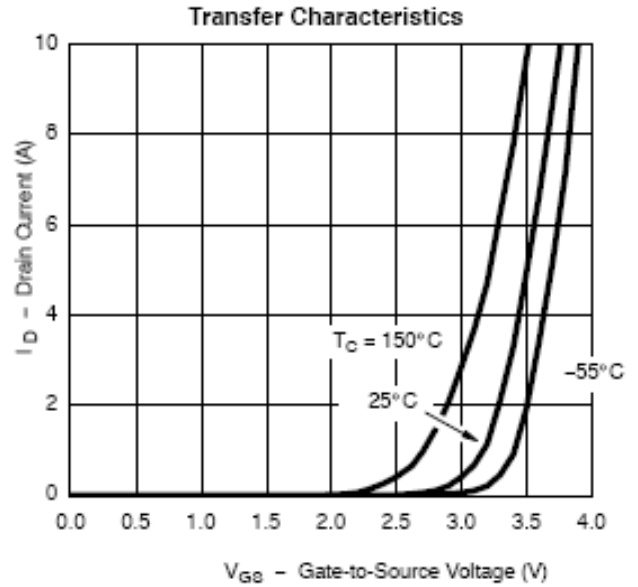
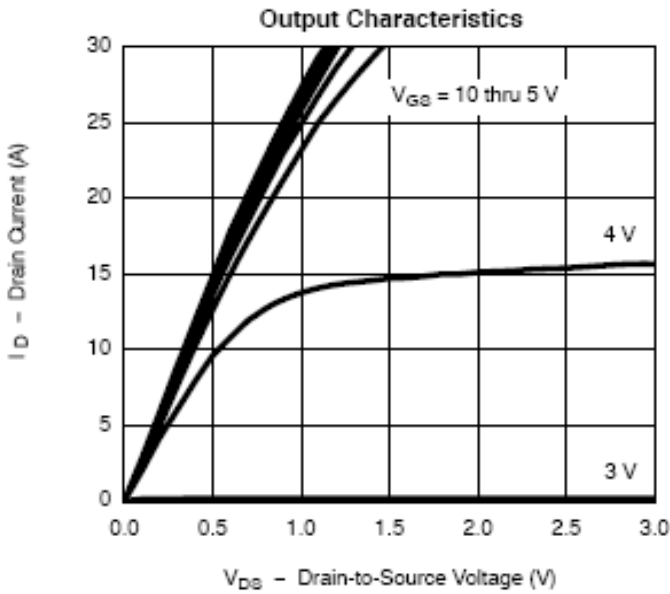
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.8		2.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$			1	uA
		$V_{DS}=60V, V_{GS}=0V$ $T_J=85^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	30			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=12A$		0.038	0.045	Ω
		$V_{GS}=4.5V, I_D=8A$		0.042	0.050	
Forward Transconductance	g_{fs}	$V_{DS}=15V, I_D=5.3A$		24		S
Diode Forward Voltage	V_{SD}	$I_S=2.0A, V_{GS}=0V$		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=30V, V_{GS}=5V$ $I_D=5.3A$		10	15	nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			3.6		
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V$ $f=1MHz$		890		pF
Output Capacitance	C_{oss}			85		
Reverse Transfer Capacitance	C_{rss}			48		
Turn-On Time	$t_{d(on)}$	$V_{DD}=30V, R_L=6.8\Omega$ $I_D=4.4A, V_{GEN}=10V$ $R_G=1\Omega$		10	15	nS
	t_r			12	20	
Turn-Off Time	$t_{d(off)}$			25	35	
	t_f			10	15	



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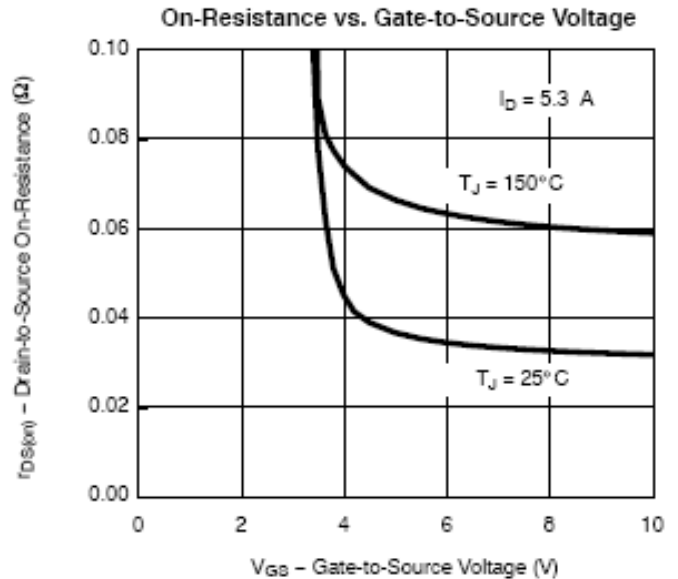
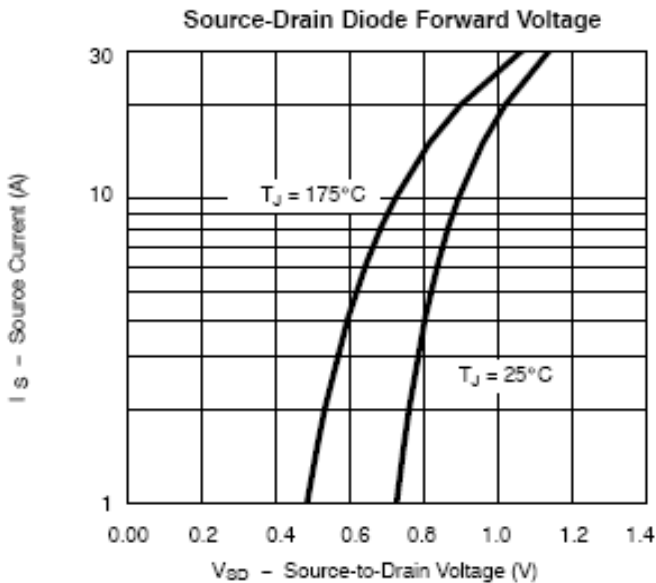
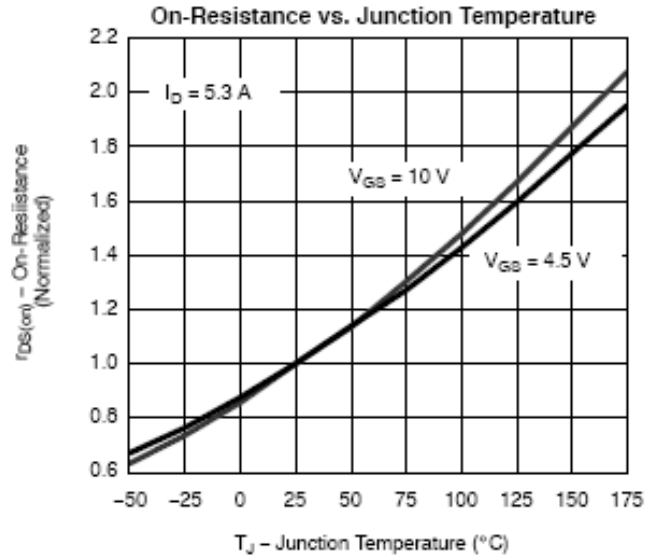
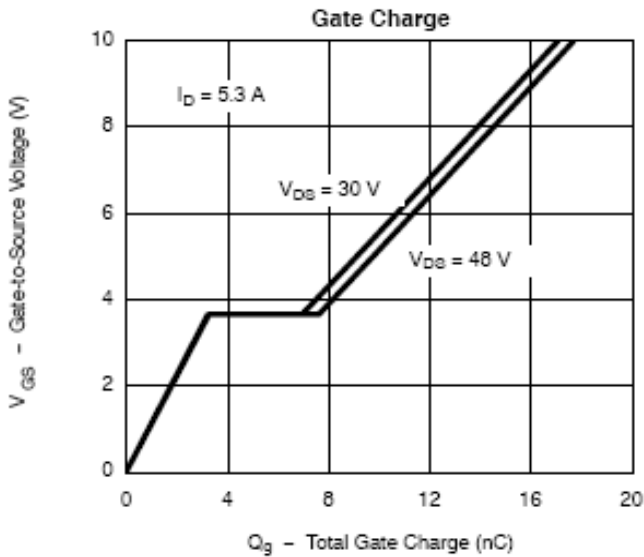
TYPICAL CHARACTERISTICS





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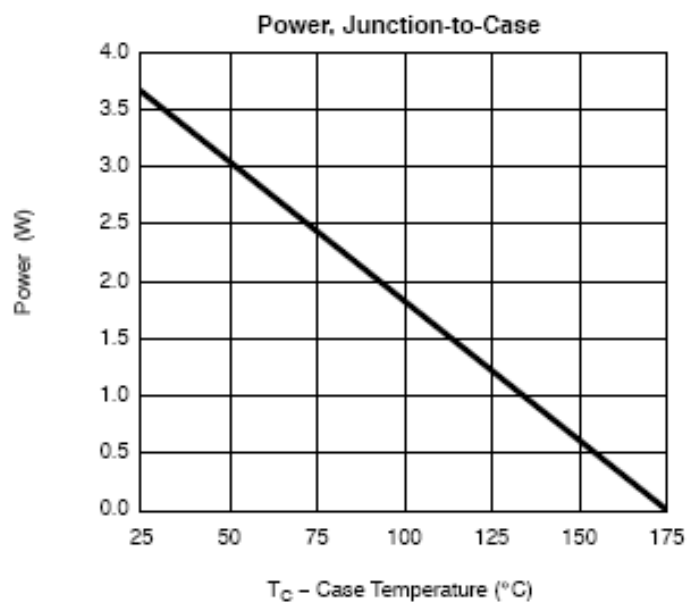
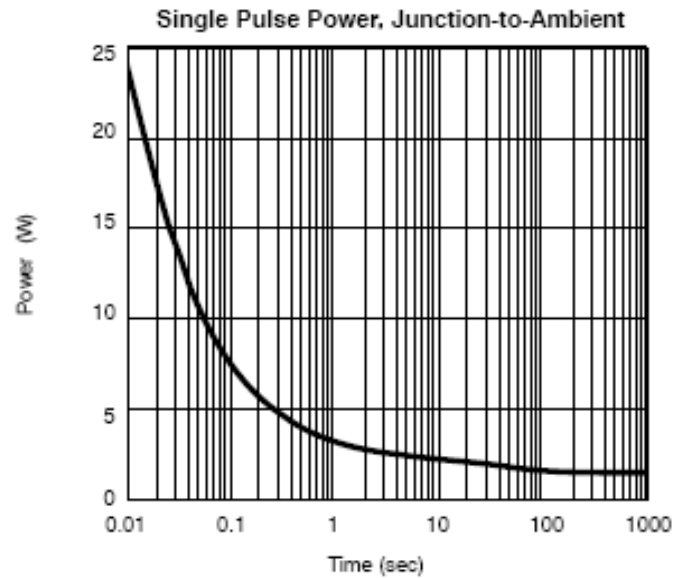
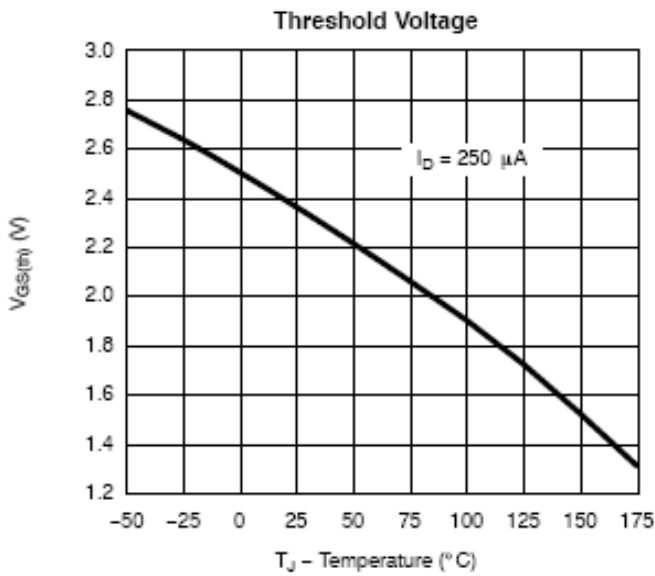
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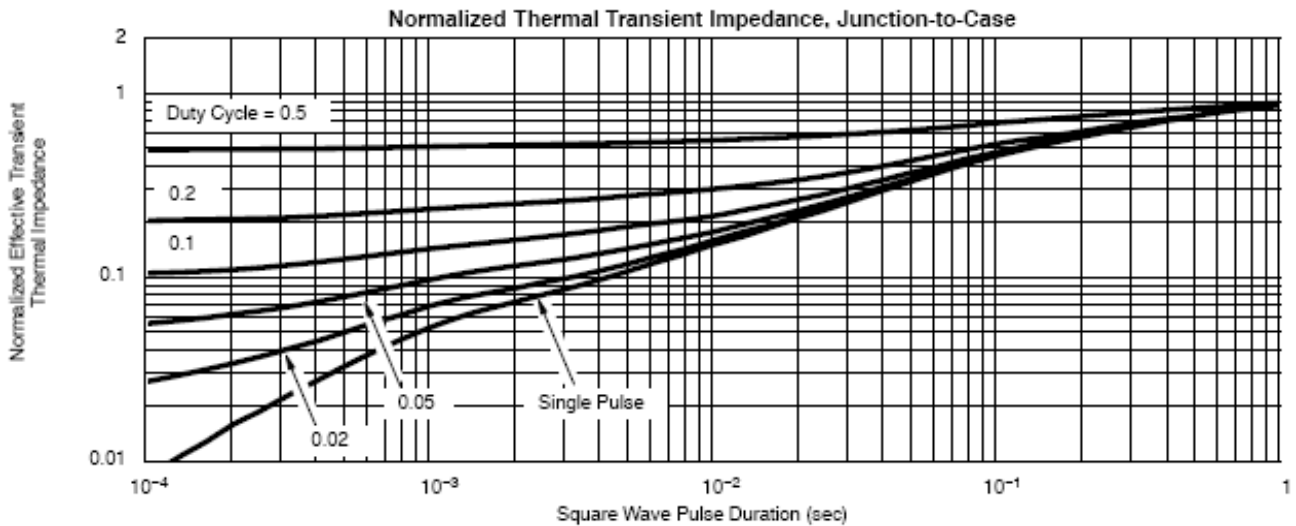
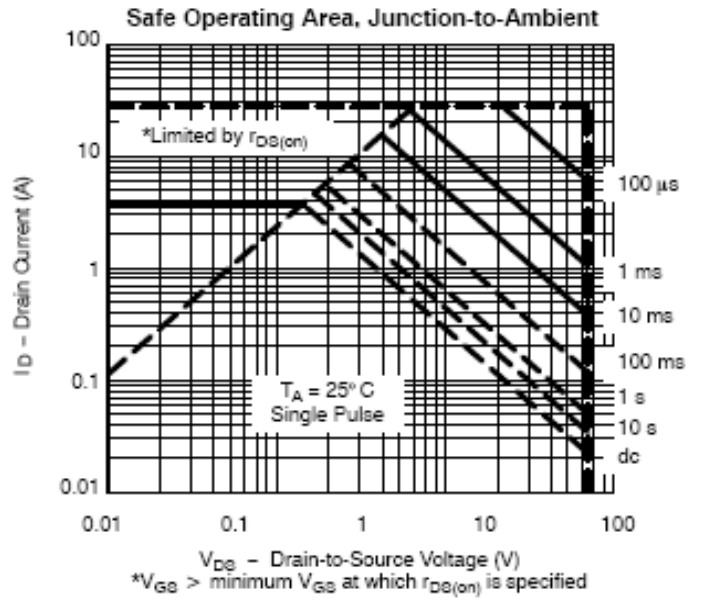
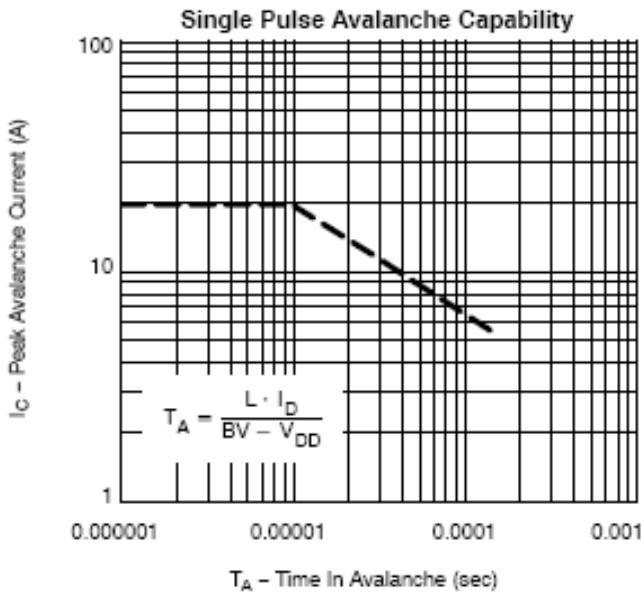
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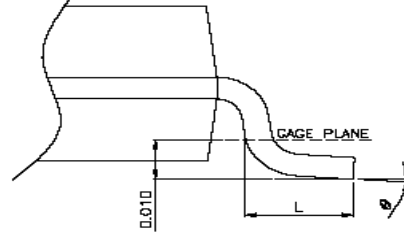
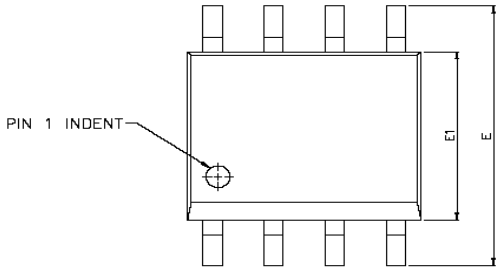
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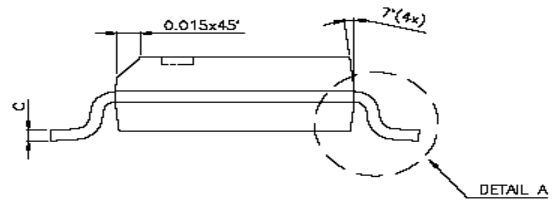
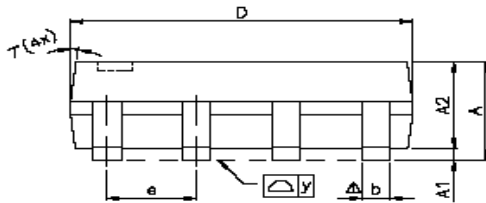


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SOP- 8 PACKAGE OUTLINE



DETAIL A



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
△ y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°



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