



SPN4996

Dual N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4996 is the Dual N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN4996 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

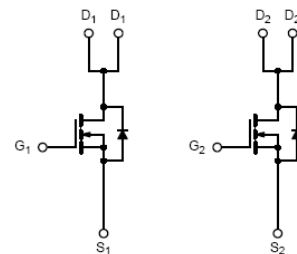
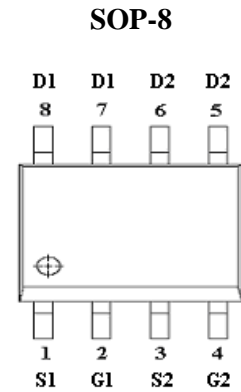
APPLICATIONS

- High Frequency Small Power Switching for MB/NB/VGA
- Network DC/DC Power System
- Load Switch
- DC/DC Converter

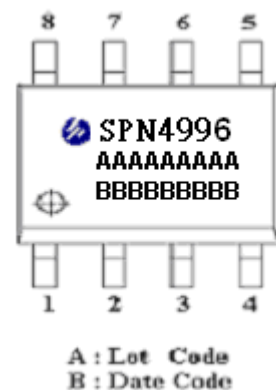
FEATURES

- ◆ 100V/3.5A, $R_{DS(ON)}=60m\Omega@V_{GS}=10V$
- ◆ 100V/3.0A, $R_{DS(ON)}=75m\Omega@V_{GS}=4.5V$
- ◆ High density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

PIN CONFIGURATION



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4996S8RGB	SOP-8	SPN4996

※ SPN4996S8RGB : 13" Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	100	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	3.5	A
		TA=70°C	2.2	
Pulsed Drain Current	I _{DM}	18	A	
Power Dissipation	P _D	2.5	W	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	80	°C/W	



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ELECTRICAL CHARACTERISTICS

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Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1		2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			10	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=125^\circ C$			100	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	3.5			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=3.5A$			60	mΩ
		$V_{GS}=4.5V, I_D=3A$			75	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=3A$		68		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=4.5V$ $I_D=3.5A$		55		nC
Gate-Source Charge	Q_{gs}			7.5		
Gate-Drain Charge	Q_{gd}			7		
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		3850		pF
Output Capacitance	C_{oss}			137		
Reverse Transfer Capacitance	C_{rss}			82		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, I_D=1A,$ $V_{GEN}=10V, R_G=3.3\Omega$		19		nS
	t_r			4		
Turn-Off Time	$t_{d(off)}$			84		
	t_f			5		



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TYPICAL CHARACTERISTICS

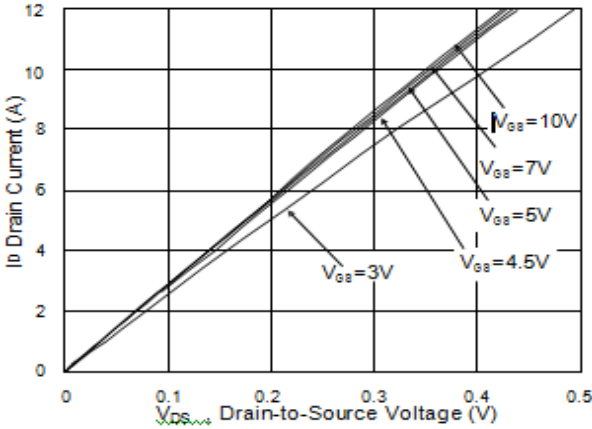


Fig. 1 Typical Output Characteristics

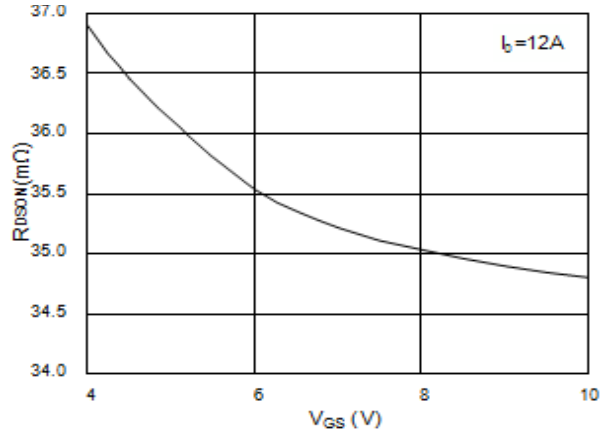


Fig. 2 On-Resistance vs. Gate Voltage

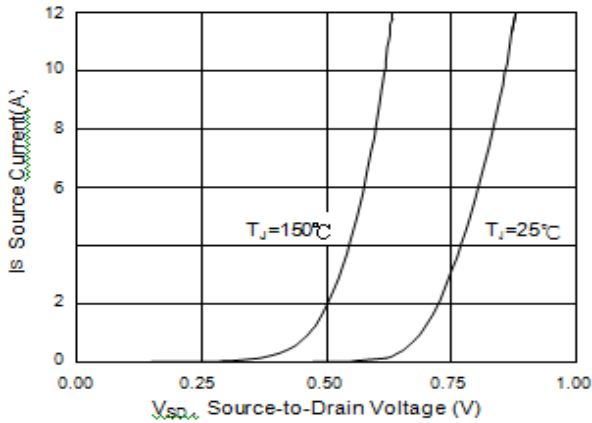


Fig. 3 Forward Characteristics of Reverse Diodes

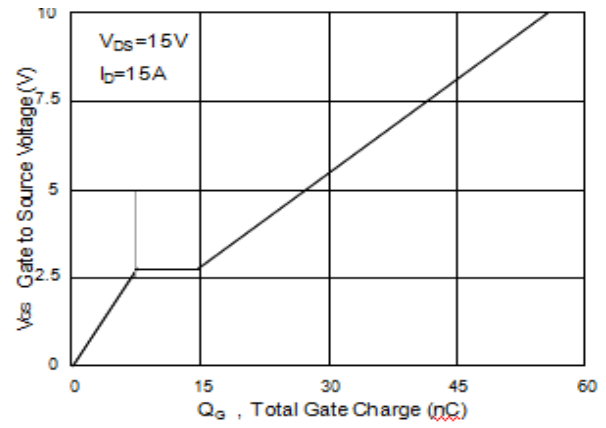


Fig. 4 Gate Charge Characteristics

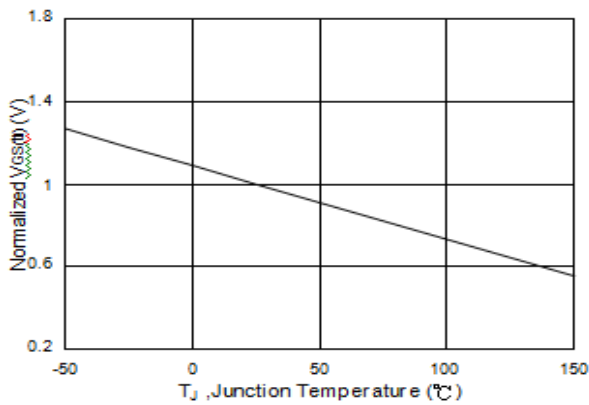


Fig. 5 Vgs vs. Junction Temperature

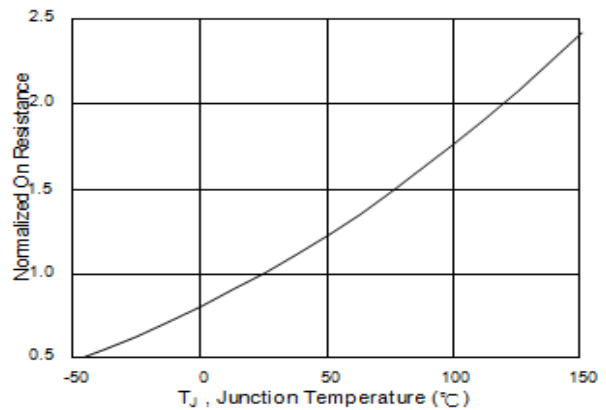


Fig. 6 On-resistance vs. Junction Temperature



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TYPICAL CHARACTERISTICS

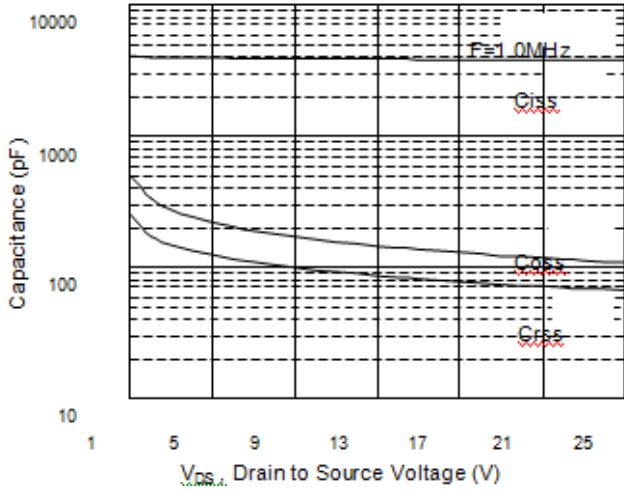


Fig. 7 Typical Capacitance Characteristics

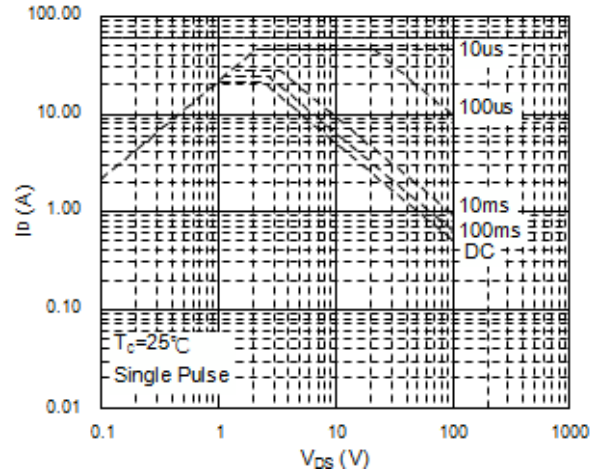


Fig. 8 Maximum Safe Operation Area

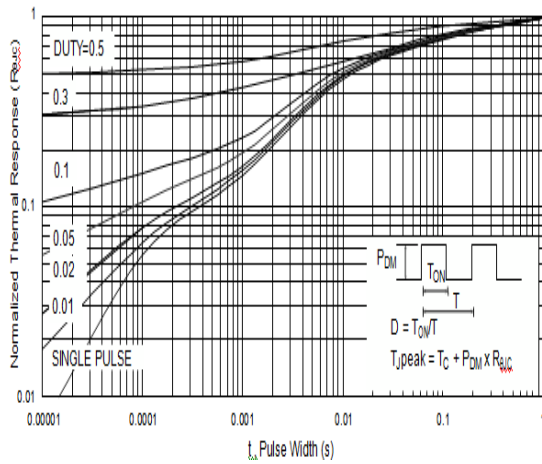


Fig. 9 Effective Transient Thermal Impedance

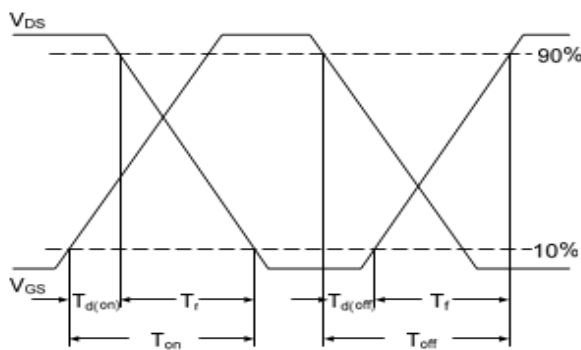


Fig. 10 Switching Time Waveform

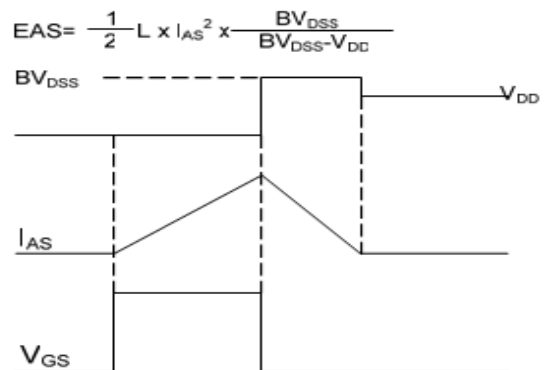


Fig. 11 Unclamped Inductive Waveform



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