



SPN5003 N-Channel Enhancement Mode MOSFET

DESCRIPTION

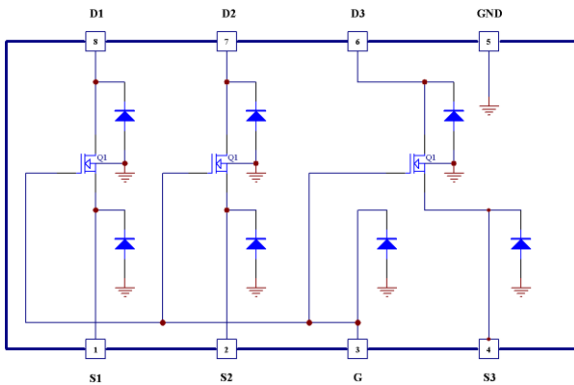
The SPN5003 is the N-Channel logic enhancement mode power field effect transistor which is produced with high voltage BiCMOS technology. This device is particularly suited for reducing the no load consumption in PC power, TV power and Adapter.

APPLICATIONS

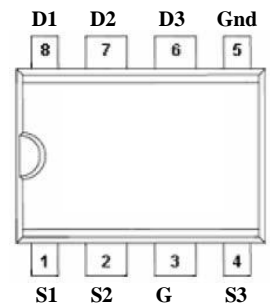
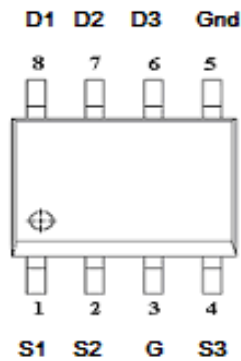
- Desk PC Power Supply
- AC adapter
- LCD TC Power Supply
-

FEATURES

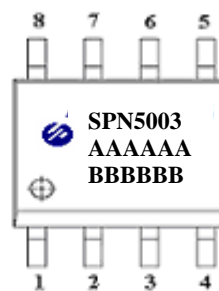
- ◆ 500V/10mA, $R_{DS(ON)}=250\Omega @ V_{GS}=10V$
- ◆ Reduce power consumption at no load for EPA/Climate Saver Application
- ◆ SOP-8 and DIP-8 package design



PIN CONFIGURATION



PART MARKING



A: Lot Code
B: Date Code

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PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	S2	Source 2
3	G	Gate
4	S3	Source 3
5	Ground	Ground
6	D3	Drain 3
7	D2	Drain 2
8	D1	Drain 1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN5003S8RGB	SOP-8	SPN5003
SPN5003D8TGB	DIP-8	SPN5003

※ SPN5003S8RGB : Tape Reel ; Pb – Free ; Halogen - Free

※ SPN5003D8TGB : Tube ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	500	V	
Gate –Source Voltage	V _{GSS}	+20	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	30	mA
		TA=70°C	20	
Pulsed Drain Current	I _{DM}	200	mA	
Power Dissipation	P _D	TA=25°C	1.3	W
		TA=70°C	1.0	
Operating Junction Temperature	T _J	150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	80	°C/W	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

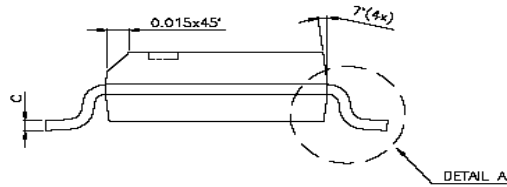
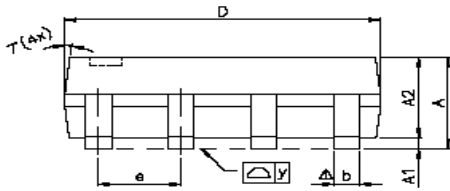
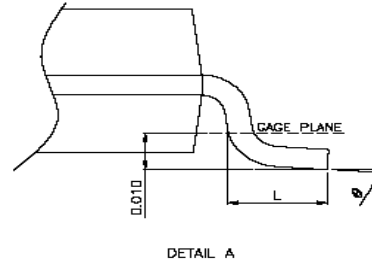
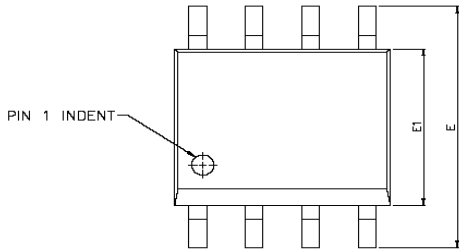
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=40\mu A$	500			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.75	1.3	2.25	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=+20V$			20	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=400V, V_{GS}=0V$			25	μA
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS} = 10V$	25			mA
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 10mA$		160	250	Ω
		$V_{GS} = 5.0V, I_D = 10mA$		180	250	Ω
Diode Forward Voltage	V_{SD}	$I_S = 10mA, V_{GS} = 0V$		0.8	1.0	V
Dynamic						
Gate-Source Charge	Q_{gs}	$V_{DS}=50V, V_{GS}=10V$ $I_D = 25mA$		1		nC
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, R_L=2.7\Omega$ $V_{GEN}=5V, R_G=3\Omega$		20		nS
	t_r			16		
Turn-Off Time	$t_{d(off)}$			4		
	t_f			3.8		



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SOP-8 PACKAGE OUTLINE

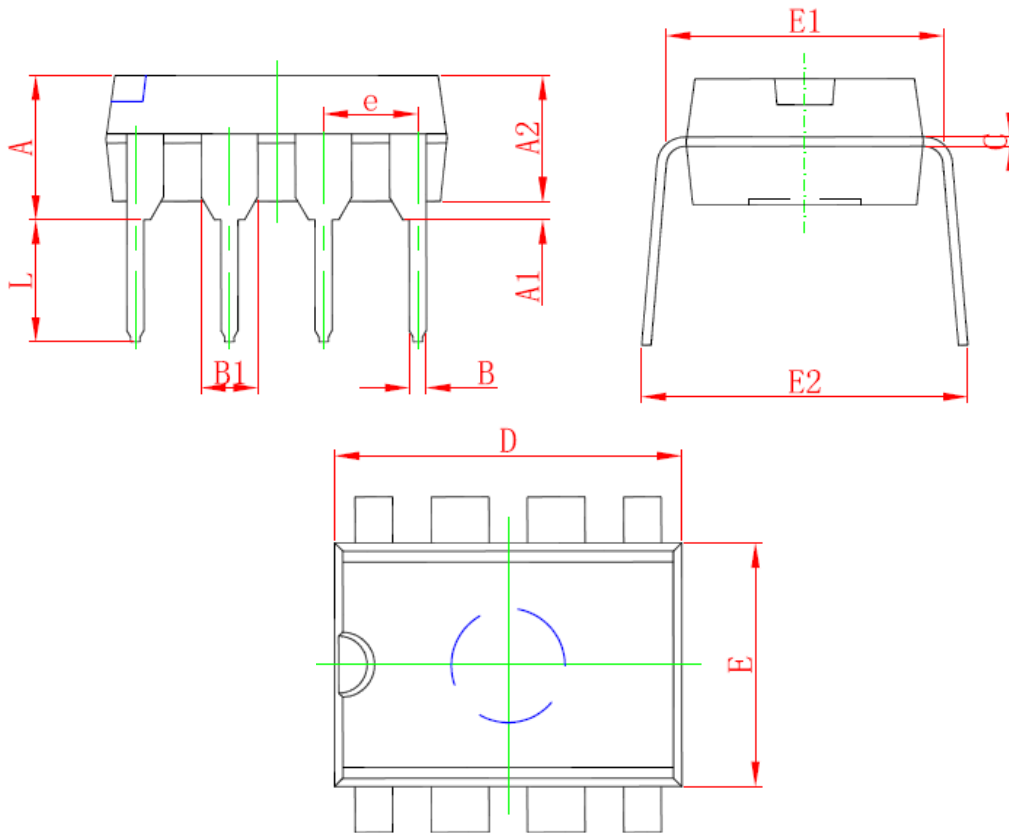


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
Ø	0°	—	8°	0°	—	8°



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DIP-8P PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354



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