SPN55T20
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN55T20 is the N-Channel enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

APPLICATIONS

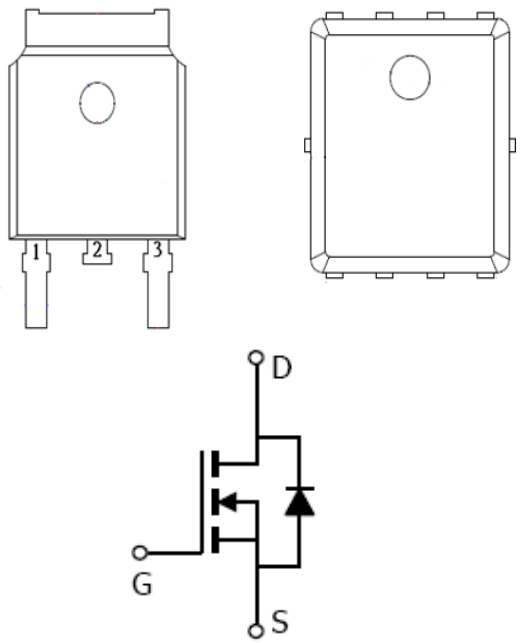
- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

FEATURES

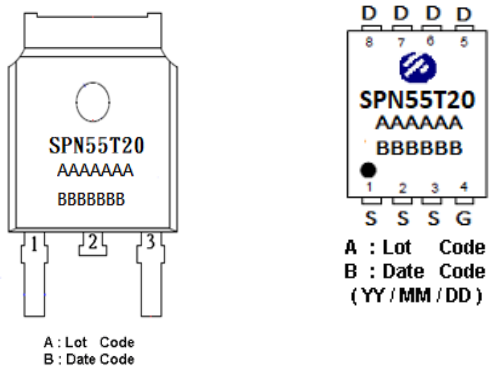
- 200V/42A,$R_{DS(ON)}$=32mΩ@V_{GS}=10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252-2L/PPAK5x6-8L package design

PIN CONFIGURATION(PPAK5x6-8L)

TO-252-2L **PPAK5x6-8L**



PART MARKING



PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PPAK5x6 PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN55T20T252RGB	TO-252-2L	SPN55T20
SPN55T20DN8RGB	PPAK5x6-8L	SPN55T20

※ SPN55T20T252RGB : Tape Reel ; Pb – Free ; Halogen – Free
※ SPN55T20DN8RGB : 13” Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	200	V
Gate–Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	T_C=25℃	I_D	42	A
	T_C=100℃		26	
Pulsed Drain Current		I_{DM}	140	A
Avalanche Energy, Single Pulse (L=0.4mH,T_C=25℃)		E_{AS}	180	mJ
Power Dissipation (TO-252)	T_C=25℃	P_D	93	W
Power Dissipation (PPAK5x6)	T_C=25℃		83	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case (TO-252)		$R_{\theta JC}$	1.35	℃/W
Thermal Resistance-Junction to Case (PPAK5x6)		$R_{\theta JC}$	1.5	℃/W

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2	3	4	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=160V,V_{GS}=0V T_J=25℃			1	uA
		V_{DS}=160V,V_{GS}=0V T_J=100℃			100	uA
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=10A		28	32	mΩ
Transconductance	gfs	V_{DS}=5V, I_D=10A		31		S
Gate Resistance	R_G	V_{GS}=0V, V_{DS}=Open, f=1MHz		4.6		Ω
Dynamic						
Total Gate Charge	Q_g	V_{DS}=100V,V_{GS}=10V I_D=10A		19		nC
Gate-Source Charge	Q_{gs}			7		nC
Gate-Drain Charge	Q_{gd}			2		nC
Input Capacitance	C_{iss}	V_{DS}=100V,V_{GS}=0V f=1MHz		1598		pF
Output Capacitance	C_{oss}			124		pF
Reverse Transfer Capacitance	C_{rss}			7.5		pF
Turn-On Time	$t_{d(on)}$	V_{DD}=100V, I_D=10A,V_{GS}=10V R_G=10Ω		12		nS
	t_r			17		nS
Turn-Off Time	$t_{d(off)}$			23		nS
	t_f			10		nS
Diode						
Diode Forward Voltage	V_{SD}	I_S=10A,V_{GS}=0V		0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=100V, I_F=10A, dI_F/d_t=100A/uS		90		nS
Reverse Recovery Charge	Q_{rr}			305		nC

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

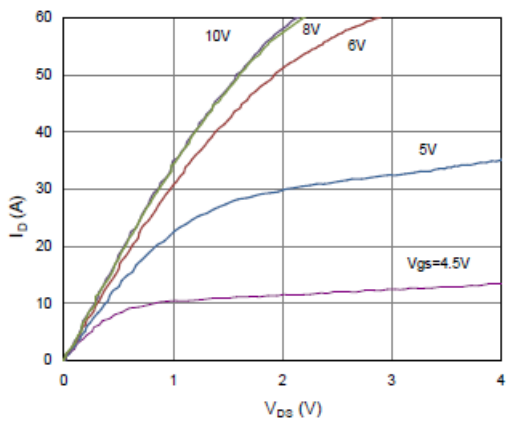


Figure 2. On-Resistance vs. Gate-Source Voltage

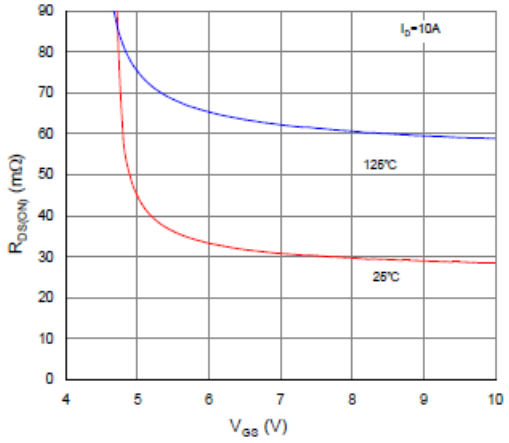


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

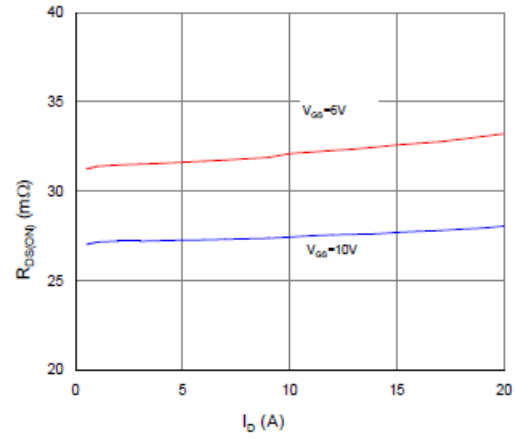


Figure 4. Normalized On-Resistance vs. Junction Temperature

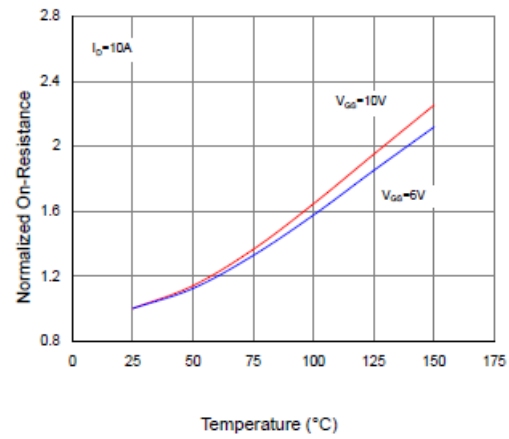


Figure 5. Typical Transfer Characteristics

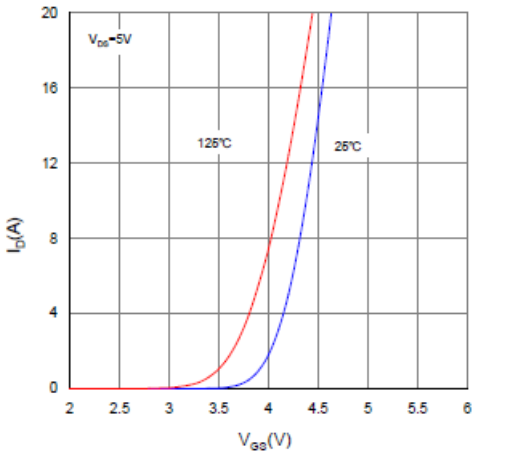
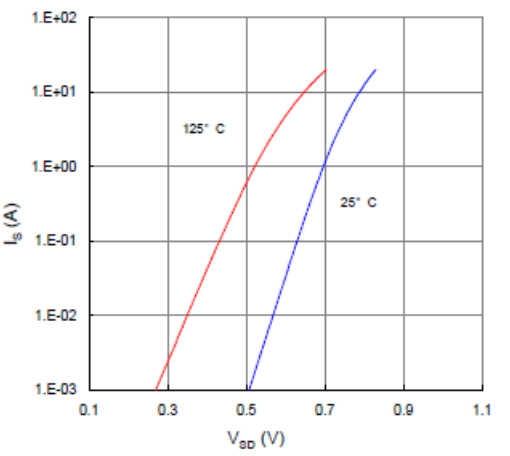


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

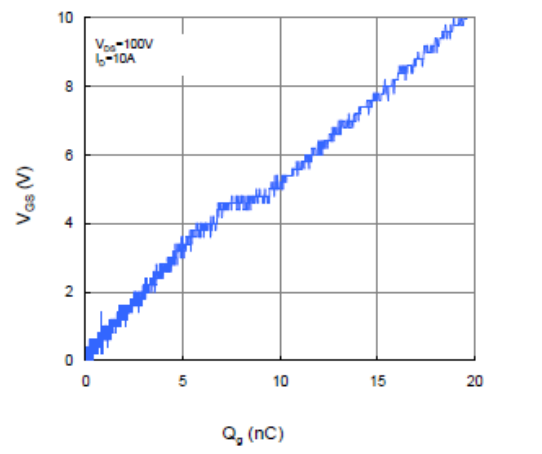


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

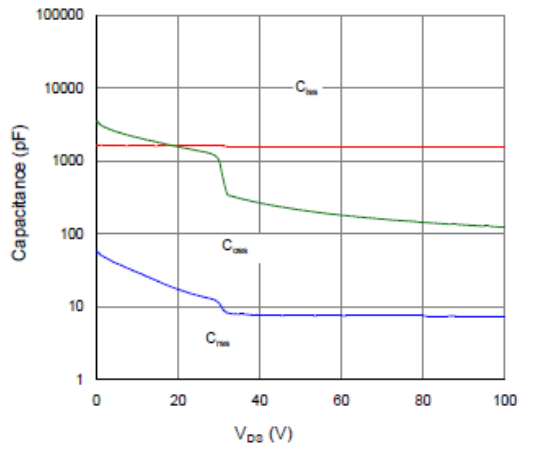


Figure 9. Maximum Safe Operating Area

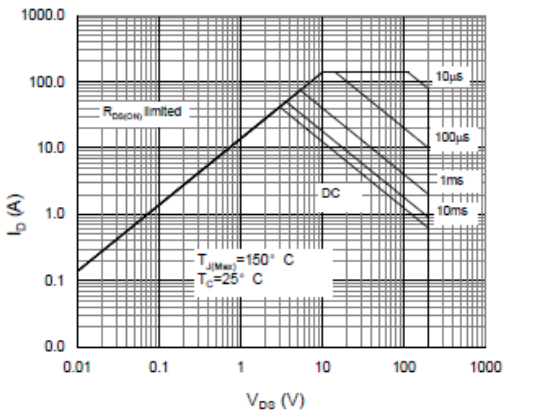


Figure 10. Maximun Drain Current vs. Case Temperature

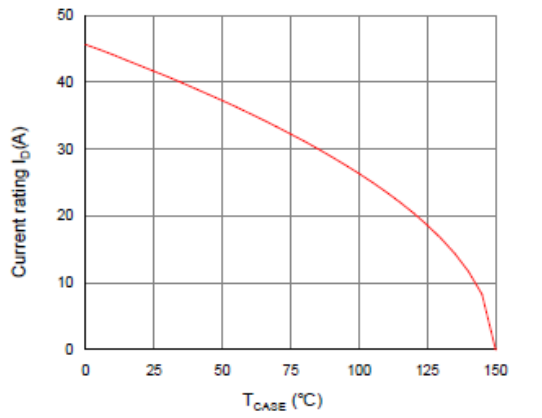
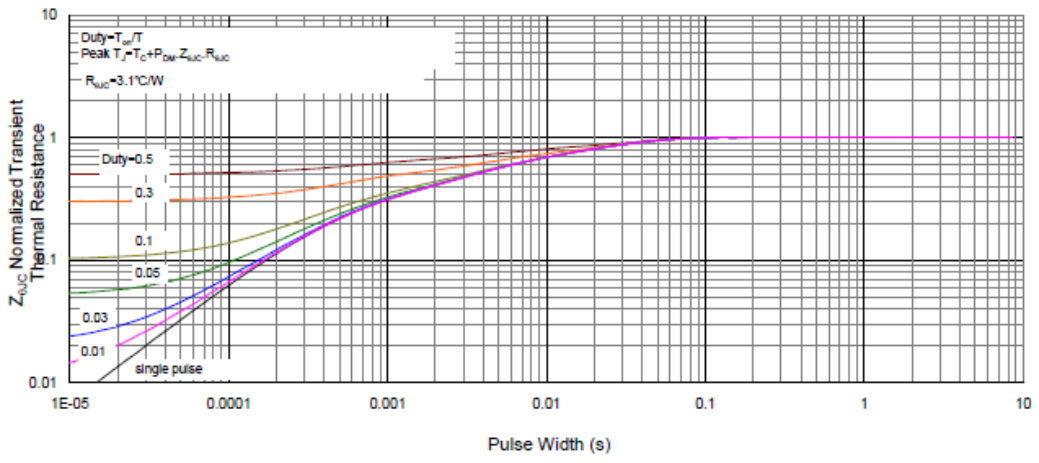


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



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