SPN6232
N-Channel Enhancement Mode MOSFET

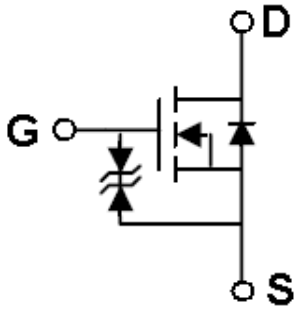
DESCRIPTION
The SPN6232 is the N-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where high-side switching, low in-line power loss, and resistance to transients are needed.

APPLICATIONS
- Drivers : Relays/Solenoids/Lamps/Hammers
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers

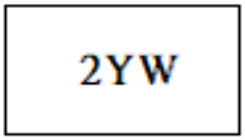
FEATURES
- N-Channel
  30V/0.95A,$R_{DS(ON)}$=400mΩ@V_{GS}=4.5V
  30V/0.75A,$R_{DS(ON)}$=500mΩ@V_{GS}=2.5V
  30V/0.65A,$R_{DS(ON)}$=650mΩ@V_{GS}=1.8V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- ESD Protected
- DFN1.0x0.6-3L(SOT-883) package design

PIN CONFIGURATION(DFN1.0x0.6-3L)

Top View



PART MARKING



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N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN6232DN3RGB	DFN1.0x0.6-3L	2

※ SPN6232DN3RGB : Tape Reel ; Pb – Free, Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate –Source Voltage		V_{GSS}	±12	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	1.2	A
	T_A=125℃		1.0	
Pulsed Drain Current (*)		I_{DM}	2.5	A
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	375	℃/W
Power Dissipation	T_A=25℃	P_D	1.35	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃

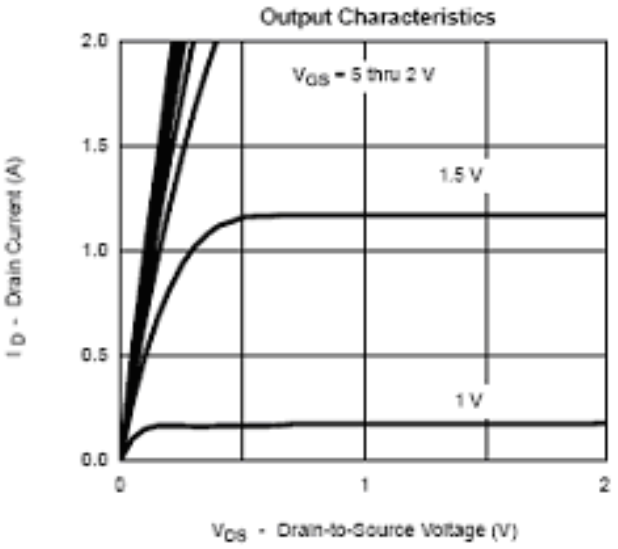
(*) Pulse width limited by safe operating area

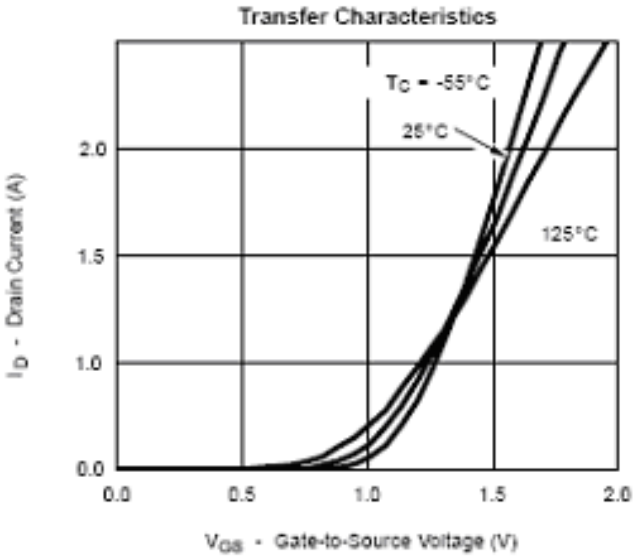
ELECTRICAL CHARACTERISTICS

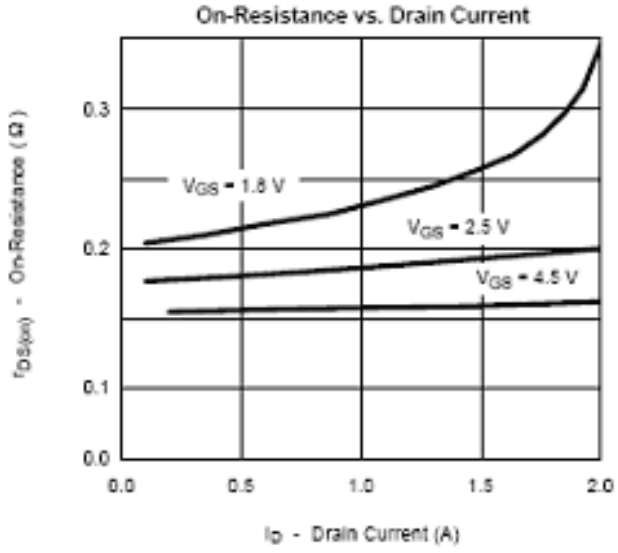
(T_A=25℃ Unless otherwise noted)

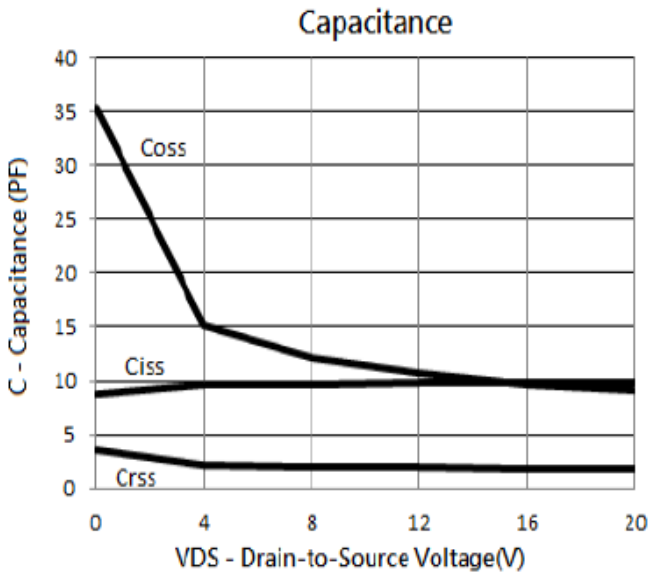
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D= 250uA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	0.45		1.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±10	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V,V_{GS}=0V,T_J=25℃			1	uA
		V_{DS}=24V,V_{GS}=0V,T_J=55℃			100	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥ 4.5V,V_{GS} =5V	0.7			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=4.5V,I_D=0.95A		0.26	0.40	Ω
		V_{GS}=2.5V,I_D=0.75A		0.38	0.50	
		V_{GS}=1.8V,I_D=0.65A		0.52	0.65	
Forward Transconductance	gfs	V_{DS}=10V,I_D=0.4A		1.0		S
Diode Forward Voltage	V_{SD}	I_S=0.15A,V_{GS}=0V		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=10V,V_{GS}=4.5V, I_D=0.6A		1.2	1.5	nC
Gate-Source Charge	Q_{gs}			0.2		
Gate-Drain Charge	Q_{gd}			0.3		
Input Capacitance	C_{iss}	V_{DS}=10V,f=1MHz,V_{GS}=0V		7.2		pF
Output Capacitance	C_{oss}			13.5		
Reverse Transfer Capacitance	C_{rss}			1.6		
Turn-On Time	$t_{d(on)}$	V_{DD}=10V,R_L=10Ω , I_D=0.5A,V_{GEN}=4.5V ,R_G=6Ω		5	10	nS
	t_r			8	15	
Turn-Off Time	$t_{d(off)}$			10	18	
	t_f			1.2	2.8	

TYPICAL CHARACTERISTICS









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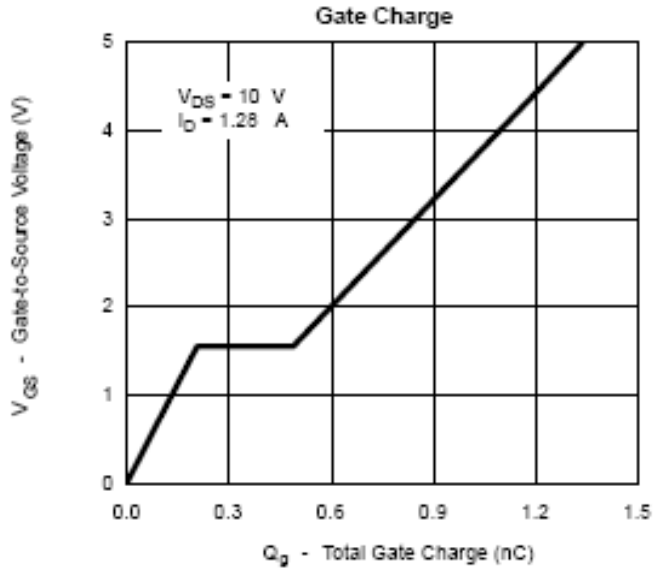

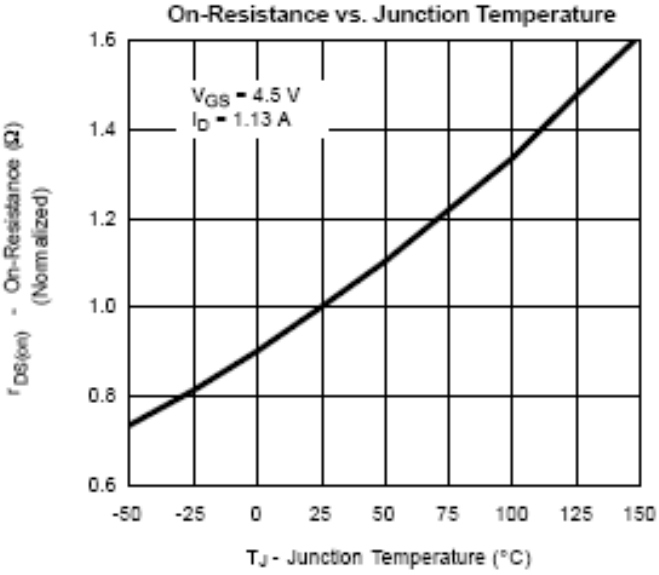

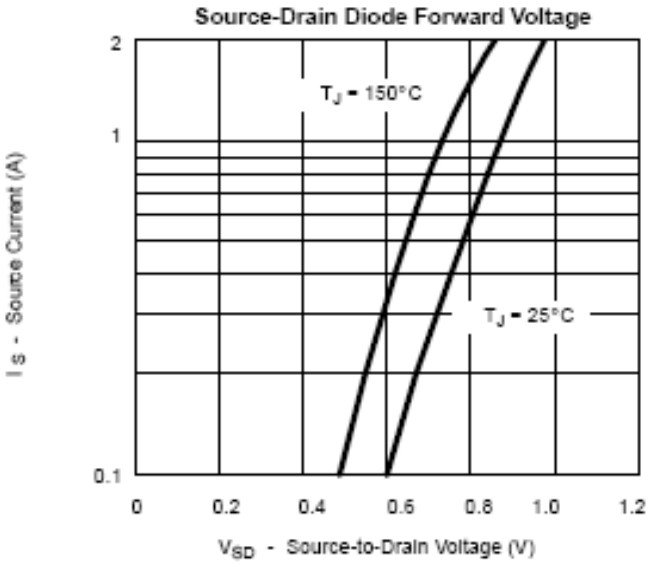

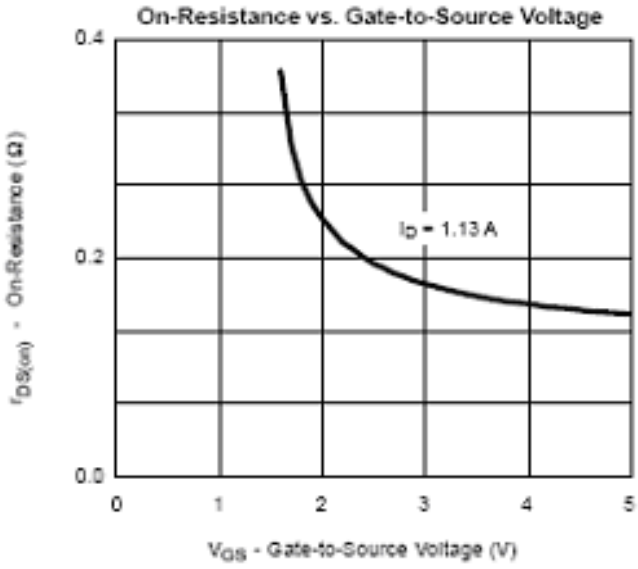

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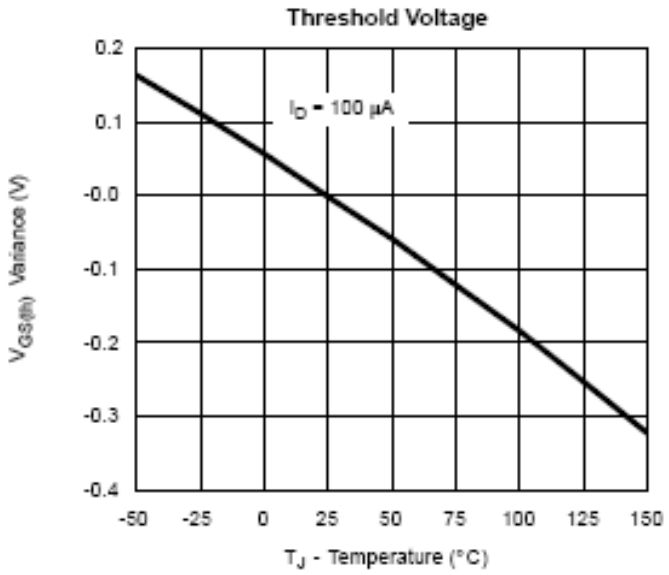

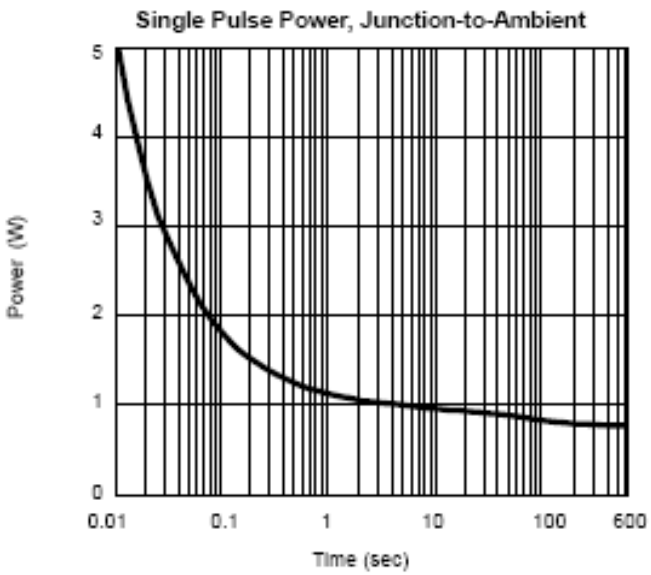

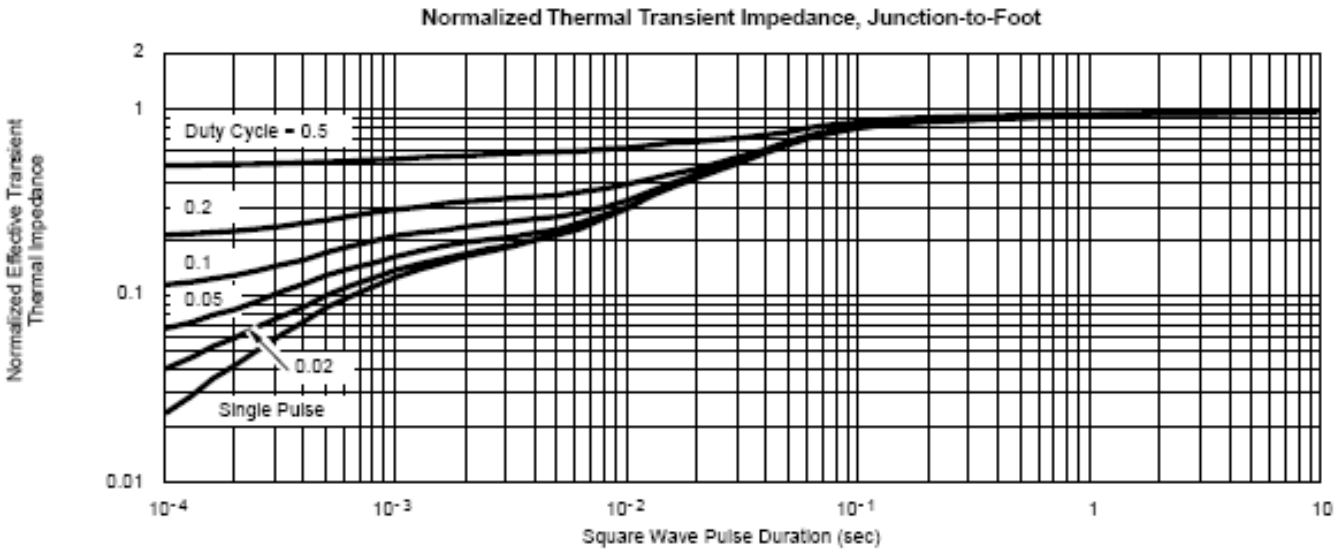

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