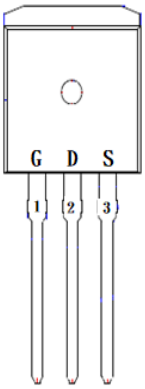
SPN80N10
N-Channel Enhancement Mode MOSFET

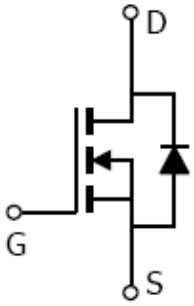
DESCRIPTION
The SPN80N10 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN80T10 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS
- AC/DC Synchronous Rectifier
- Load Switch
- UPS
- Motor Control
- Power Tool

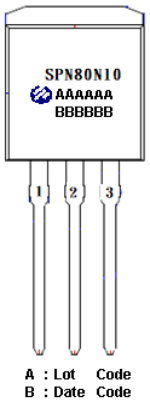
FEATURES
- 100V/73A, $R_{DS(ON)}$=8.0mΩ@V_{GS}=10V
- High density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-262-3L package design

PIN CONFIGURATION
TO-262-3L





PART MARKING



SPN80N10
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN80N10T263TGB	TO-262-3L	SPN80N10

※ SPN80N10T263TGB : Tube ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	T_C=25℃	I_D	73	A
	T_C=100℃		46	
Pulsed Drain Current		I_{DM}	260	A
Avalanche Energy, Single Pulse, L=0.1mH		E_{AS}	245	mJ
Power Dissipation@ T_A=25℃ (TO-262-3L)		P_D	104	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case (TO-262-3L)		$R_{\theta JC}$	0.85	℃/W

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2.0		4.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	VDS=80VGS=0V T_J=25℃			1	uA
		VDS=80VGS=0V T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		6.5	8.0	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		60		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS}=Open, f=1MHz		1.3		Ω
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=50V,V_{GS}=10V I_D=20A		32		nC
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			4		
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V f=1MHz		1876		pF
Output Capacitance	C_{oss}			348		
Reverse Transfer Capacitance	C_{rss}			5.6		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V,R_L=1Ω I_D=20A,V_{GS}=10V R_G=10Ω		7		nS
	t_r			4		
Turn-Off Time	$t_{d(off)}$			20		
	t_f			3		

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

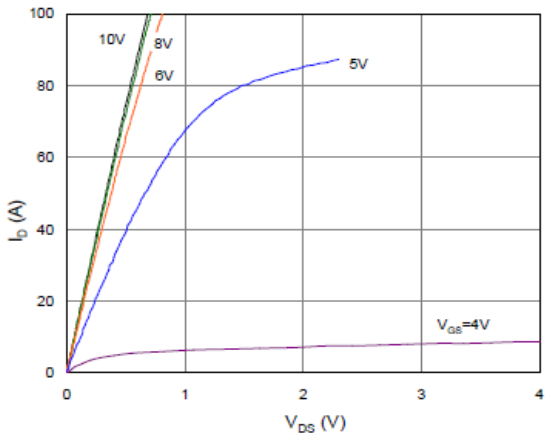


Figure 2. On-Resistance vs. Gate-Source Voltage

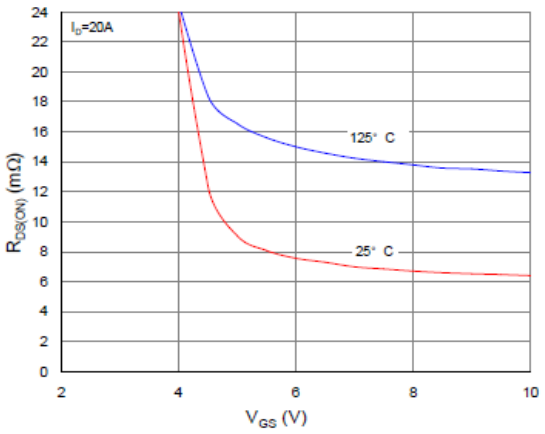


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

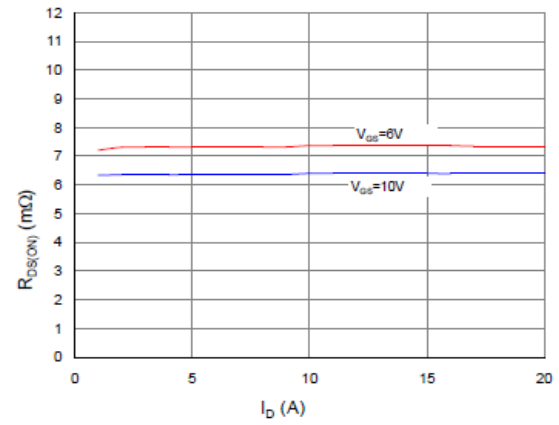


Figure 4. Normalized On-Resistance vs. Junction Temperature

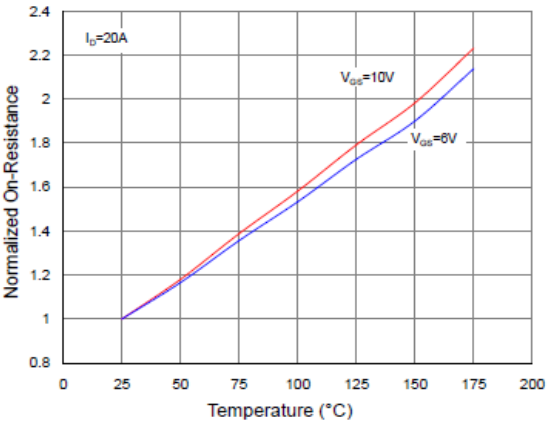


Figure 5. Typical Transfer Characteristics

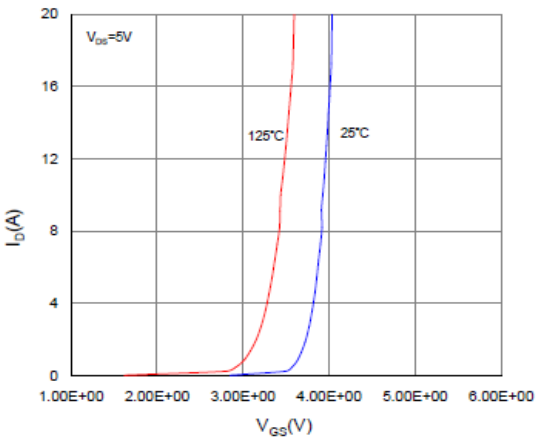
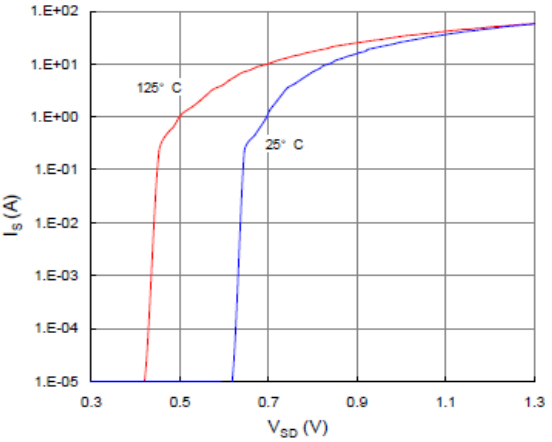


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

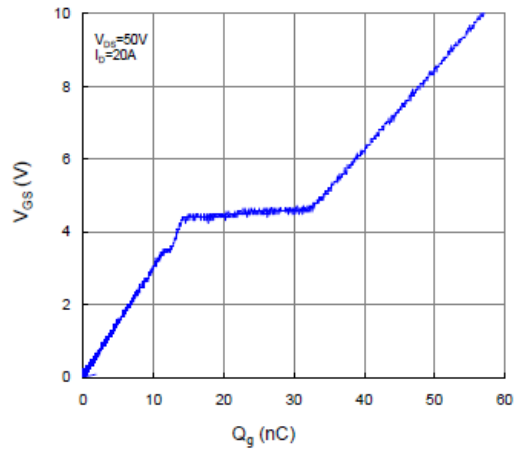


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

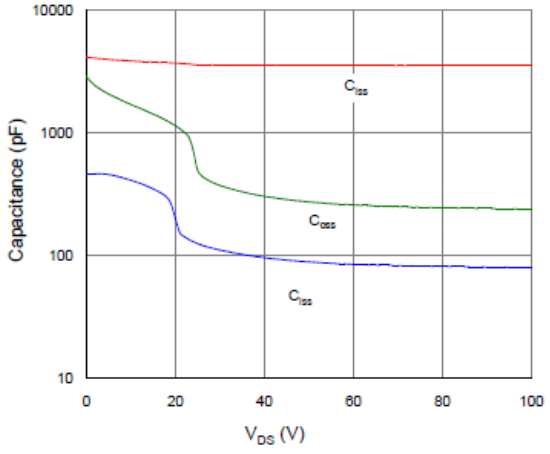


Figure 9. Maximum Safe Operating Area

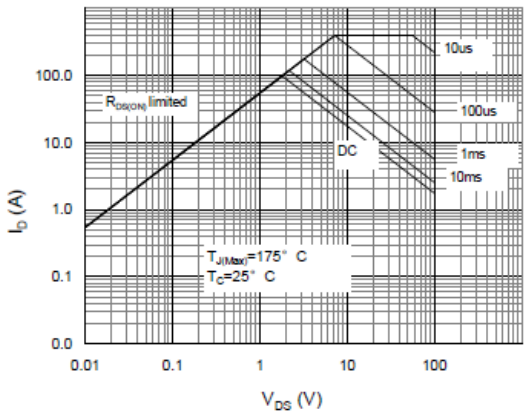


Figure 10. Maximun Drain Current vs. Case Temperature

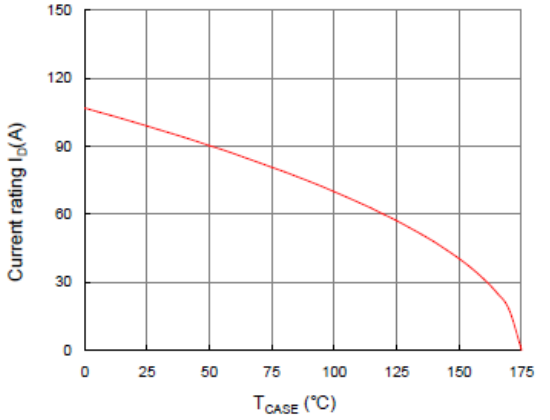
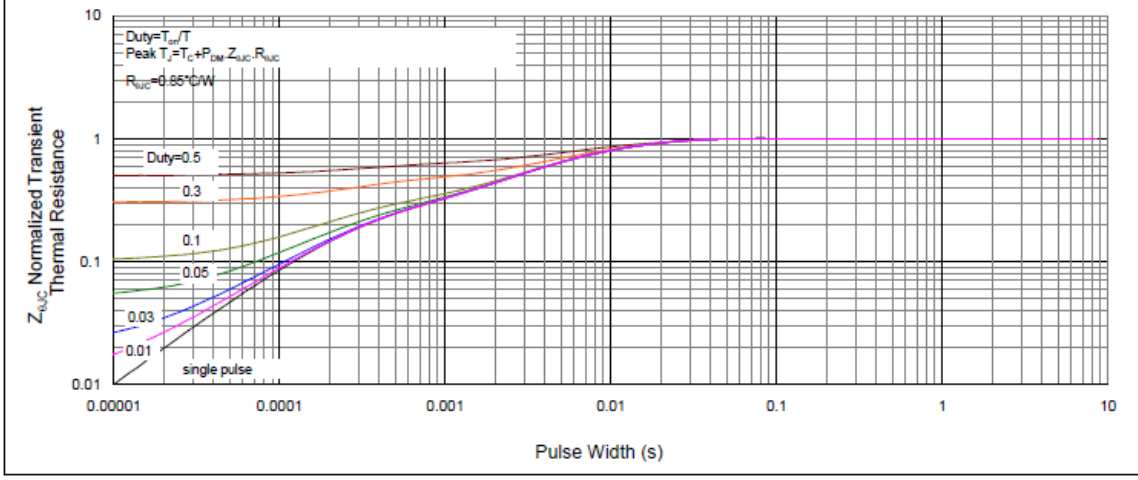
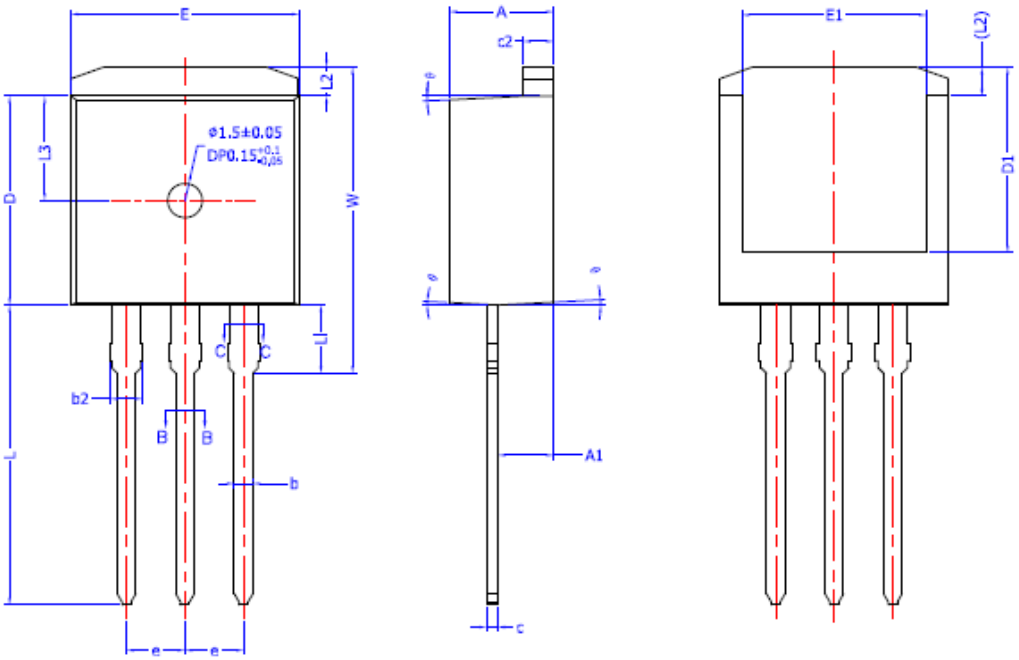
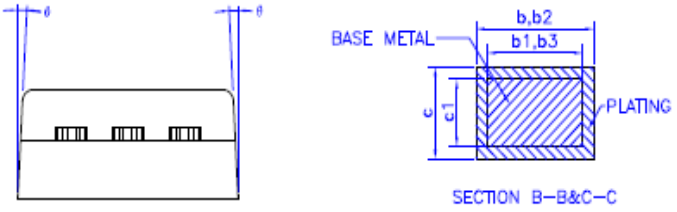


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



TO-262-3L PACKAGE OUTLINE





COMMON DIMENSIONS
(UNITS OF MEASURE =MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	2.20	2.40	2.60
b	0.76	—	0.89
b1	0.75	0.80	0.85
b2	1.23	—	1.37
b3	1.22	1.27	1.32
c	0.47	—	0.60
c1	0.46	0.51	0.56
c2	1.25	1.30	1.35
D	9.10	9.20	9.30
D1	8.00	—	--
E	9.80	9.90	10.00
E1	7.80	—	--
e	2.54 BSC		
L	12.90	13.20	13.50
L1	2.80	3.00	3.20
L2	1.17	1.27	1.40
L3	4.60 REF		
W	13.25	—	14.00
θ	1°	3°	5°

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