



SPN80T06

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN80T06 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

- ◆ 60V/80A, $R_{DS(ON)}=9m\Omega@V_{GS}=10V$
60V/80A, $R_{DS(ON)}=13m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L/PPAK5x6-8L package design

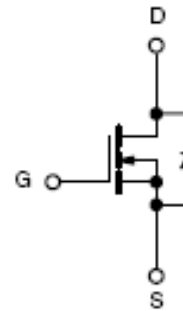
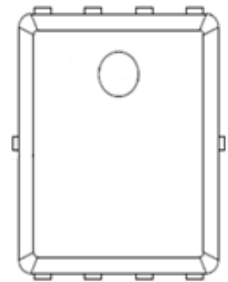
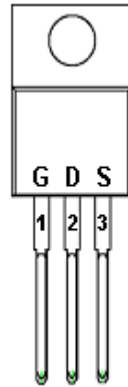
APPLICATIONS

- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

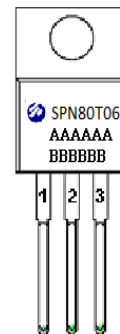
PIN CONFIGURATION

TO-220-3L

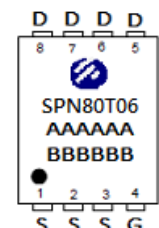
PPAK5x6



PART MARKING



AAAAA: Wafer lot no
BBBBBB: date code



A : Lot Code
B : Date Code
(YY/MM/DD)



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TO-220-3L PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PPAK5x6-8L PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN80T06T220TGB	TO-220-3L	SPN80T06
SPN80T06DN8RGB	PDFN5x6-8L	SPN80T06

※ SPN80T06T220TGB : Tube ; Pb – Free ; Halogen - Free

※ SPN80T06DN8RGB : Tape&Reel ; Pb – Free ; Halogen - Free



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ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	VDSS	60	V	
Gate-Source Voltage	VGSS	±20	V	
Continuous Drain Current(TO-220-3L)	ID	TA=25°C	80	A
		TA=70°C	55	
Continuous Drain Current(PPAK5x6)	ID	TA=25°C	62	A
		TA=70°C	39	
Pulsed Drain Current	IDM	270	A	
Power Dissipation (TA=25°C)	PD	TO-220-3L	104	W
		PPAK5x6	83	
Avalanche Energy with Single Pulse (Tj=25°C, L =0.1mH)	EAS	130	mJ	
Operating Junction Temperature	TJ	-55/150	°C	
Storage Temperature Range	TSTG	-55/150	°C	
Thermal Resistance-Junction to Case (TO-220)	RθJC	1.2	°C/W	
Thermal Resistance-Junction to Case (PPAK5x6)	RθJC	1.5	°C/W	

Note :

The maximum current rating is package limited at 120A for TO-220-3L

The maximum current rating is package limited at 80A for PPAK5x6-8L



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.8	2.4	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=48V, V_{GS}=0V$ $T_J=25^\circ C$			1	uA
		$V_{DS}=48V, V_{GS}=0V$ $T_J=100^\circ C$			100	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		7.3	9	mΩ
		$V_{GS}=4.5V, I_D=20A$		10	13	
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}$ open, $f=1MHz$		1.5		Ω
Diode Forward Voltage	V_{SD}	$I_S=20A, V_{GS}=0V$		0.9	1.2	V
Dynamic						
Total Gate Charge (10V)	Q_g	$V_{DS}=30V, V_{GS}=10V$ $I_D=20A$		24		nC
Total Gate Charge (4.5V)	Q_g			12		
Gate-Source Charge	Q_{gs}			5.0		
Gate-Drain Charge	Q_{gd}			3.0		
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V$ $f=1MHz$		1620		pF
Output Capacitance	C_{oss}			415		
Reverse Transfer Capacitance	C_{rss}			3		
Turn-On Time	$t_{d(on)}$	$V_{DD}=30V, I_D=20A$ $V_{GEN}=10V, R_G=10\Omega$		9		nS
	t_r			4		
Turn-Off Time	$t_{d(off)}$			29		
	t_f			4		



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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

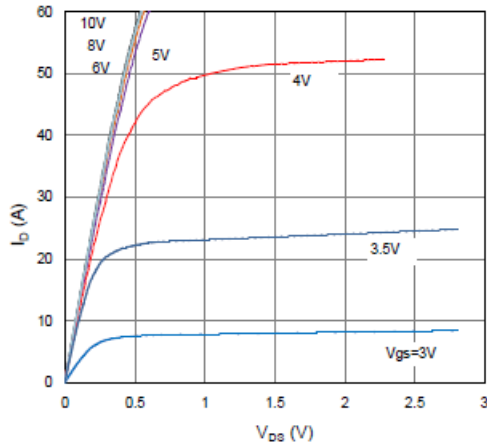


Figure 2. On-Resistance vs. Gate-Source Voltage

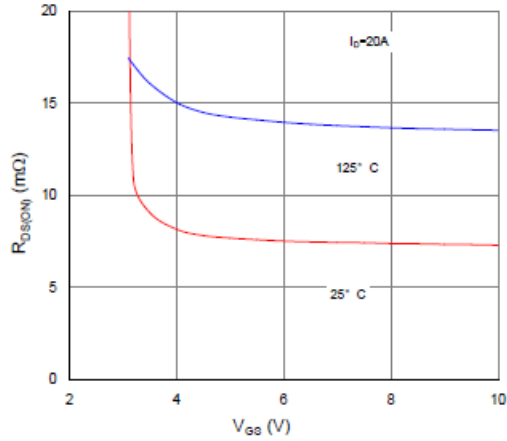


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

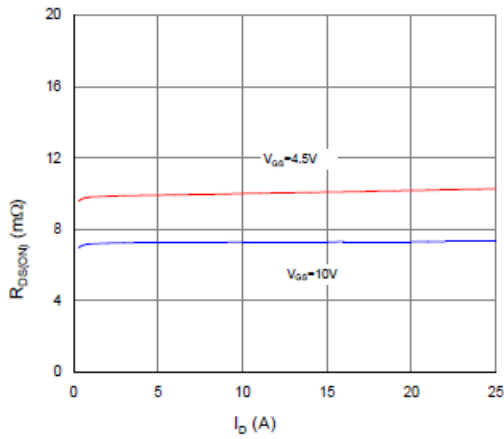


Figure 4. Normalized On-Resistance vs. Junction Temperature

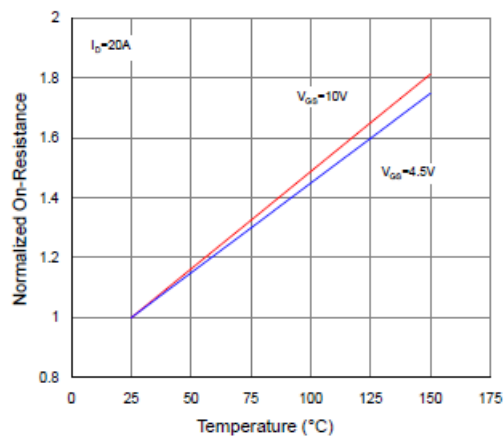


Figure 5. Typical Transfer Characteristics

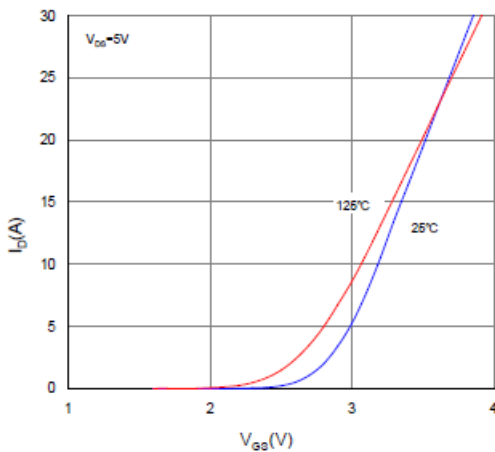
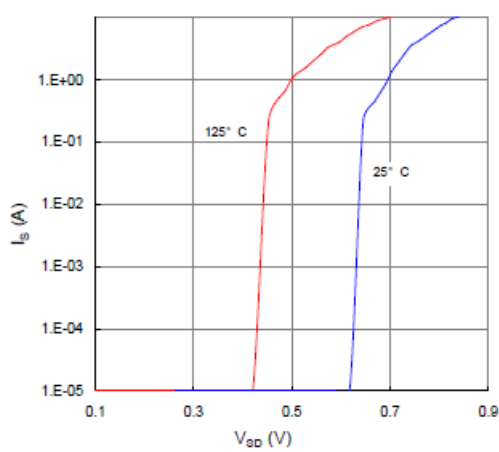


Figure 6. Typical Source-Drain Diode Forward Voltage





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TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

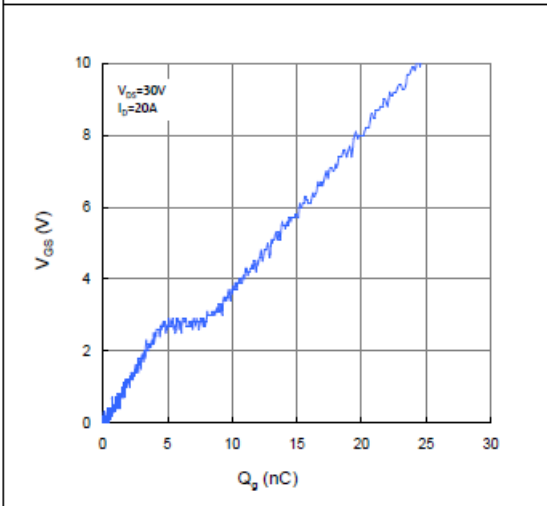


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

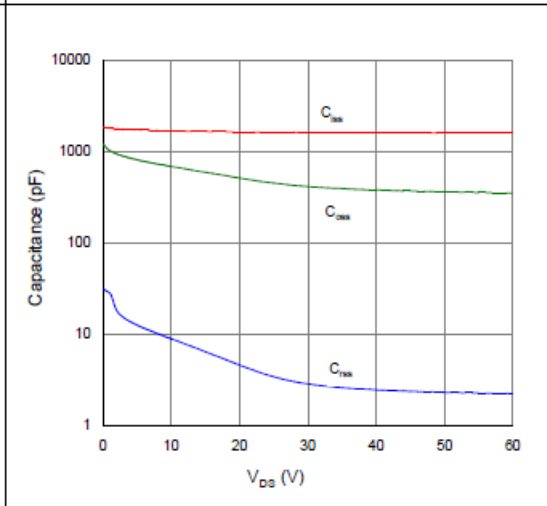


Figure 9. Maximum Safe Operating Area

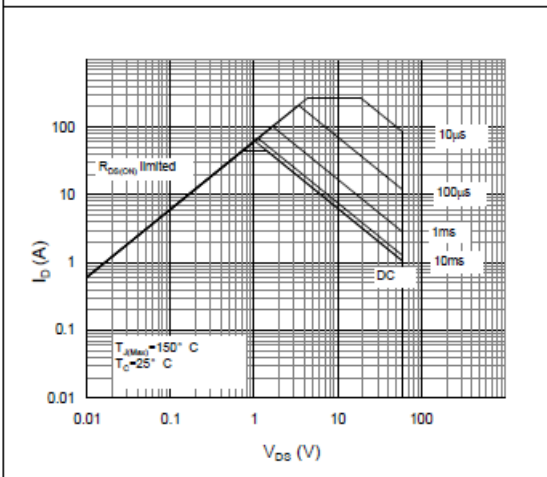


Figure 10. Maximum Drain Current vs. Case Temperature

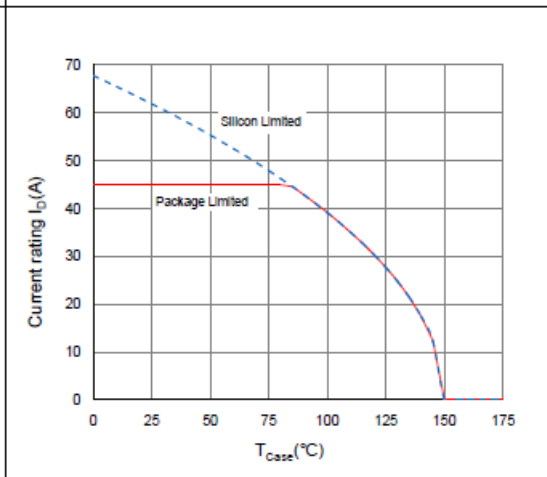
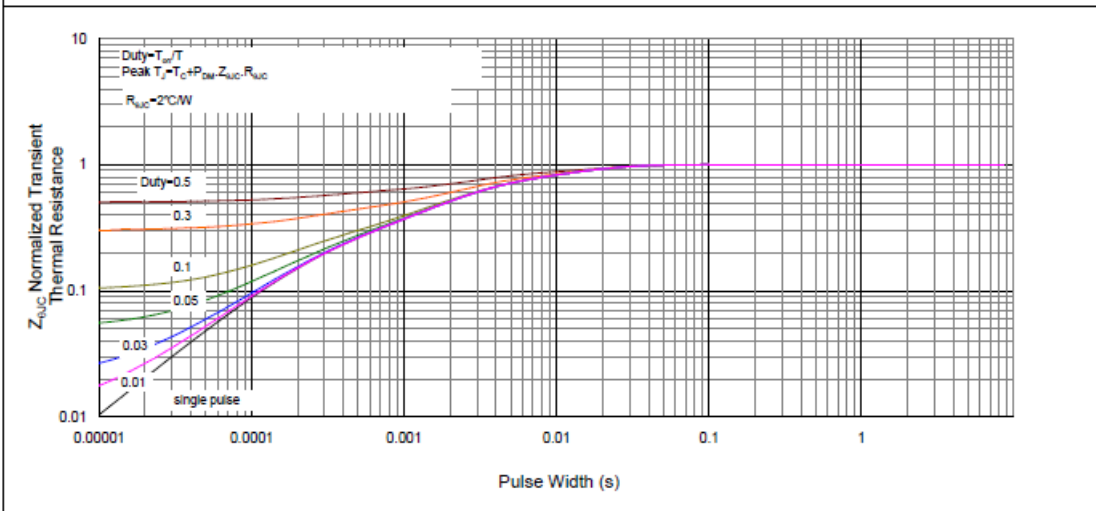


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

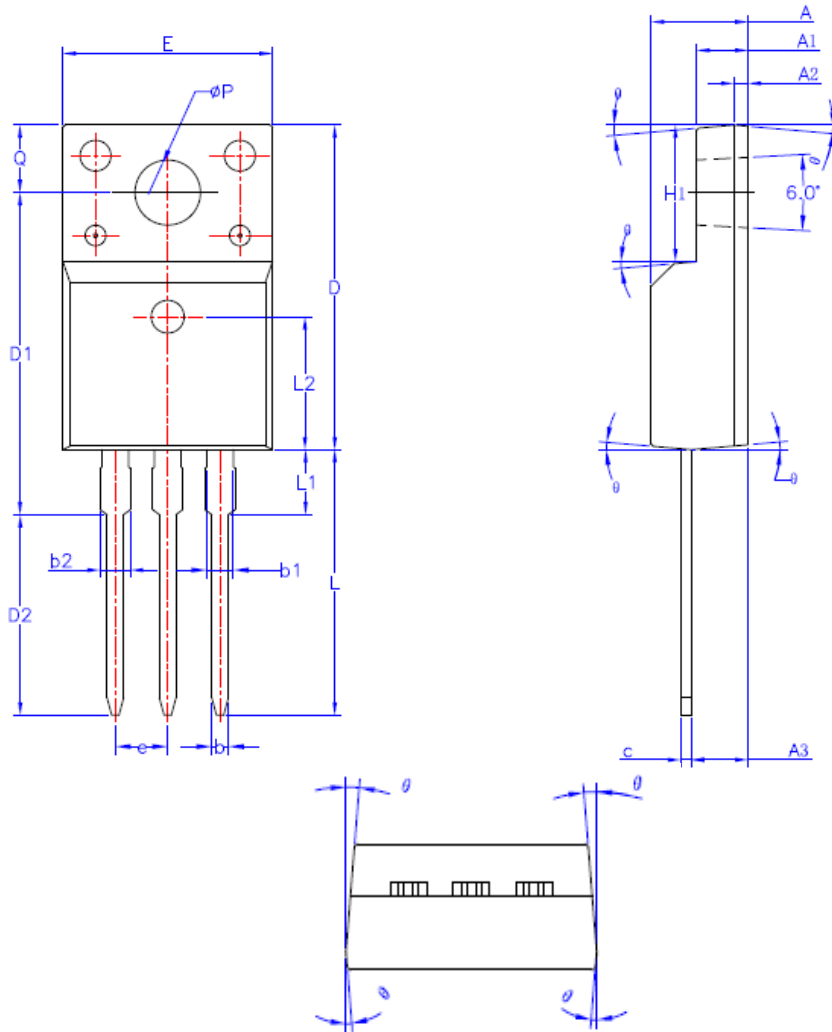




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TO-220-3L PACKAGE OUTLINE



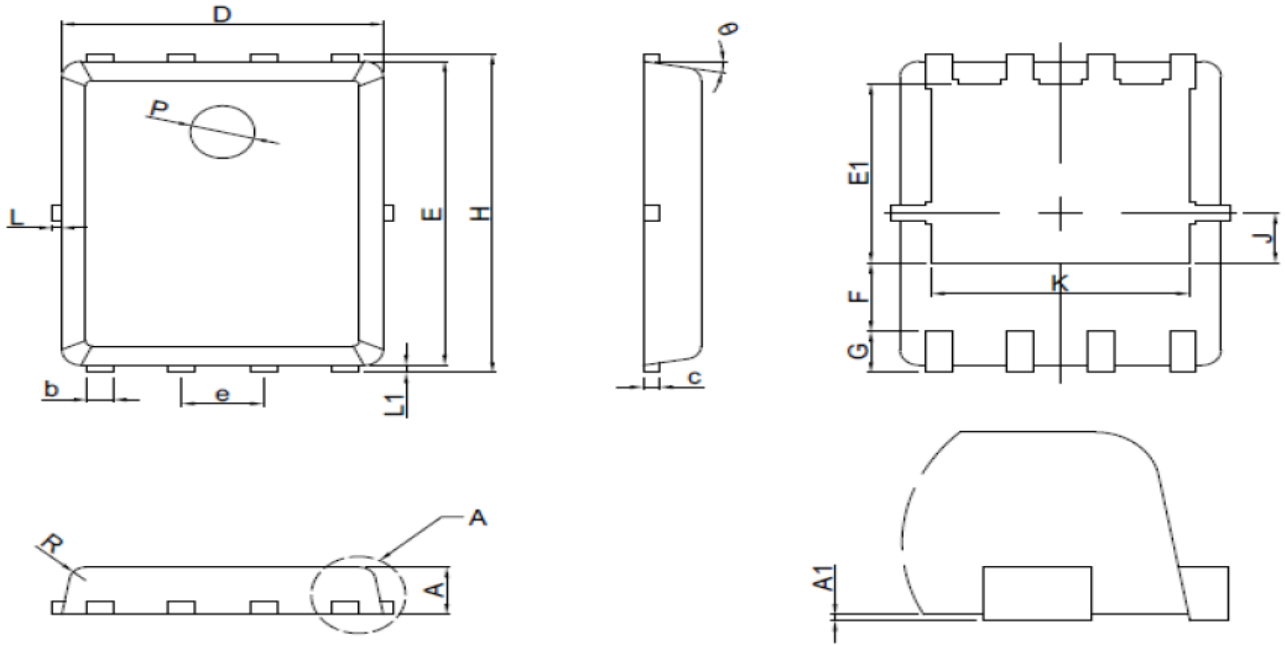
SYMBOL	MIN	NOM	MAX
A	4.50	4.70	4.83
A1	2.34	2.54	2.74
A2	0.7REF		
A3	2.56	2.76	2.93
b	0.70	--	0.90
b1	1.18	--	1.40
b2	--	--	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.55	15.75	15.95
D2	9.60	9.80	10.00
E	9.96	10.16	10.36
e	2.54BSC		
H1	6.48	6.68	6.88
L	12.68	12.98	13.28
L1	-	-	3.50
L2	6.50REF		
φ P	3.08	3.18	3.28
Q	3.20	-	3.40
θ 1	1°	3°	5°



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PPAK5X6 PACKAGE OUTLINE



SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.8	0.95	1.1
A1	0.00	0.03	0.05
b	0.33	0.41	0.51
c	0.254 REF		
D	4.80	4.95	5.10
F	1.40 REF		
E	5.70	5.80	5.90
e	1.27 BSC		
H	5.90	6.05	6.20
L1	0.06	0.13	0.20
G	0.60 REF		
J	0.95 BSC		
K	4.00 REF		
L	---	----	0.20
P	1.00 REF		
E1	3.40REF		
E2	0.95 REF		
θ	6°	10°	14°
R	0.25REF		



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