



SPN8454

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8454 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

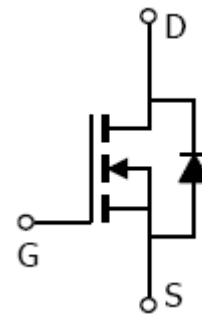
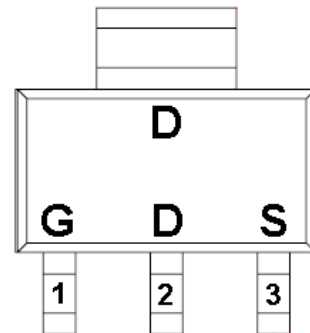
FEATURES

- ◆ 150V/2A, $R_{DS(ON)}=350m\Omega @ V_{GS}=10V$
- ◆ 150V/1A, $R_{DS(ON)}=400m\Omega @ V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-223 package design

APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

PIN CONFIGURATION(SOT-223)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8454S22RGB	SOT-223	8454

※ SPN8454S22RGB : Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current ($T_J=150^{\circ}\text{C}$)	I_D	2.8	A
Pulsed Drain Current	I_{DM}	12	A
Power Dissipation	P_D	2.8	W
		$T_C=25^{\circ}\text{C}$	
		1.1	
	$T_A=70^{\circ}\text{C}$		
Operating Junction Temperature	T_J	-55/150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^{\circ}\text{C}$
Thermal Resistance-Junction to Ambient (steady state)	$R_{\theta JA}$	42	$^{\circ}\text{C}/\text{W}$



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ELECTRICAL CHARACTERISTICS

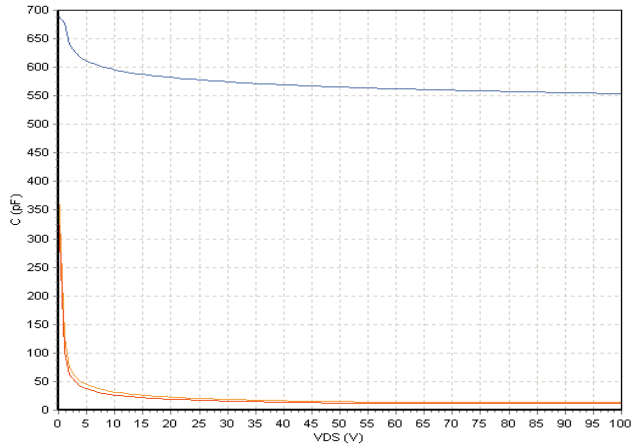
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	150			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=120V, V_{GS}=0V$ $T_J=25^\circ C$			1	uA
		$V_{DS}=120V, V_{GS}=0V$ $T_J=125^\circ C$			10	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=2A$		320	350	mΩ
		$V_{GS}=4.5V, I_D=1A$		350	400	
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=2A$		2.4		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=120V, V_{GS}=10V,$ $I_D=2A$		9	13	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			1.4		
Input Capacitance	C_{iss}	$V_{DS}=120V, V_{GS}=0V$ $f=1MHz$		508		pF
Output Capacitance	C_{oss}			29		
Reverse Transfer Capacitance	C_{rss}			16.5		
Turn-On Time	$t_{d(on)}$	$V_{DD}=120V, I_D=2A,$ $V_{GS}=10V, R_G=3.3\Omega$		2		nS
	t_r			21.5		
Turn-Off Time	$t_{d(off)}$			11.2		
	t_f			18.8		

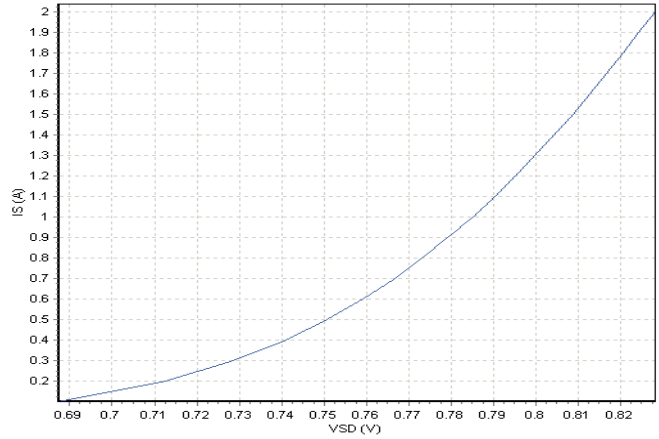


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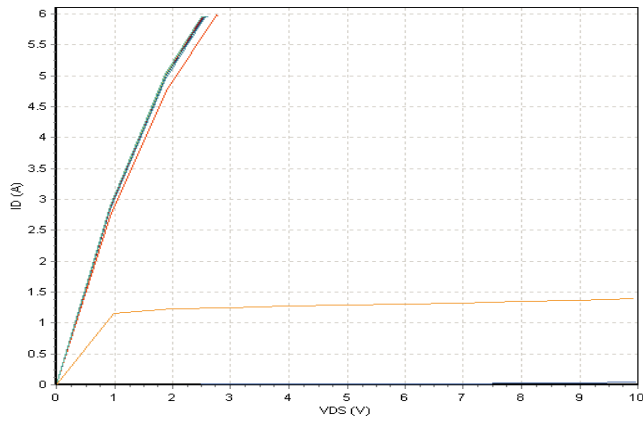
TYPICAL CHARACTERISTICS



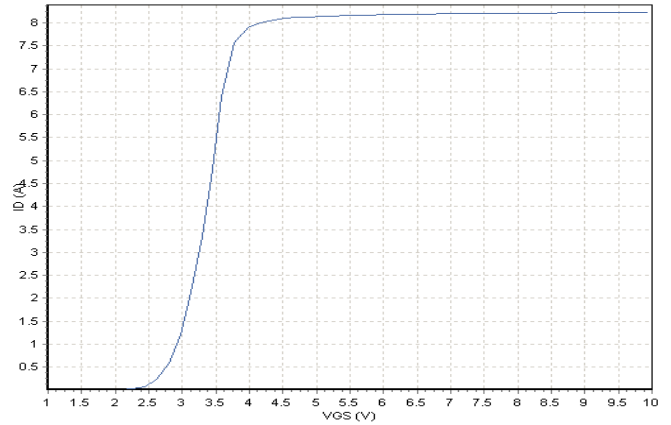
No.1 Capacitance



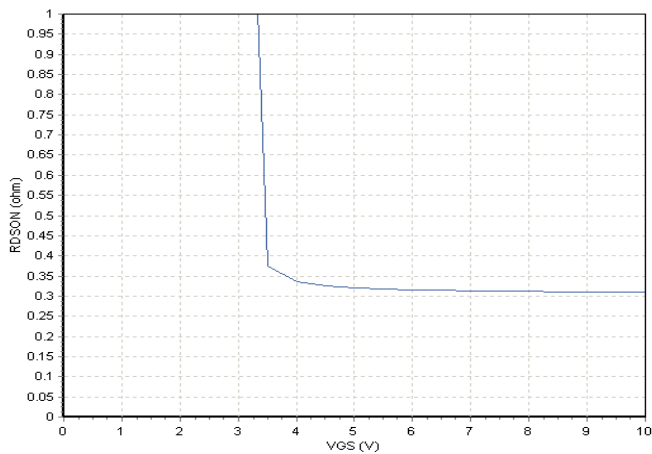
No.2 Source-Drain Diode Forward Voltage



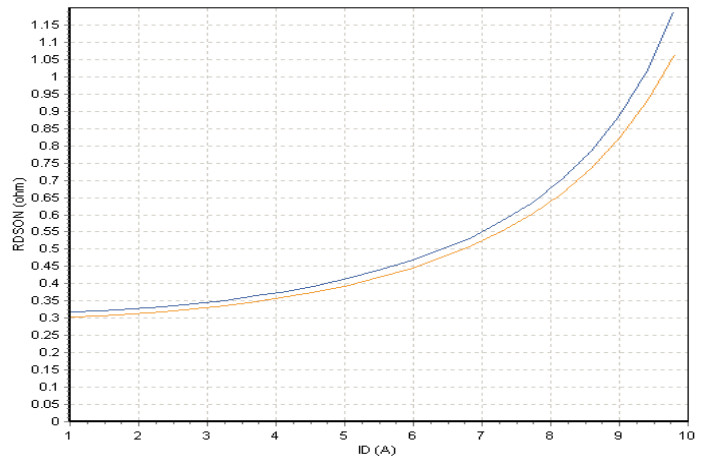
No.3 Output Characteristics



No.4 Transfer Characteristics



No.5 On-Resistance vs. Gate-to-source Voltage



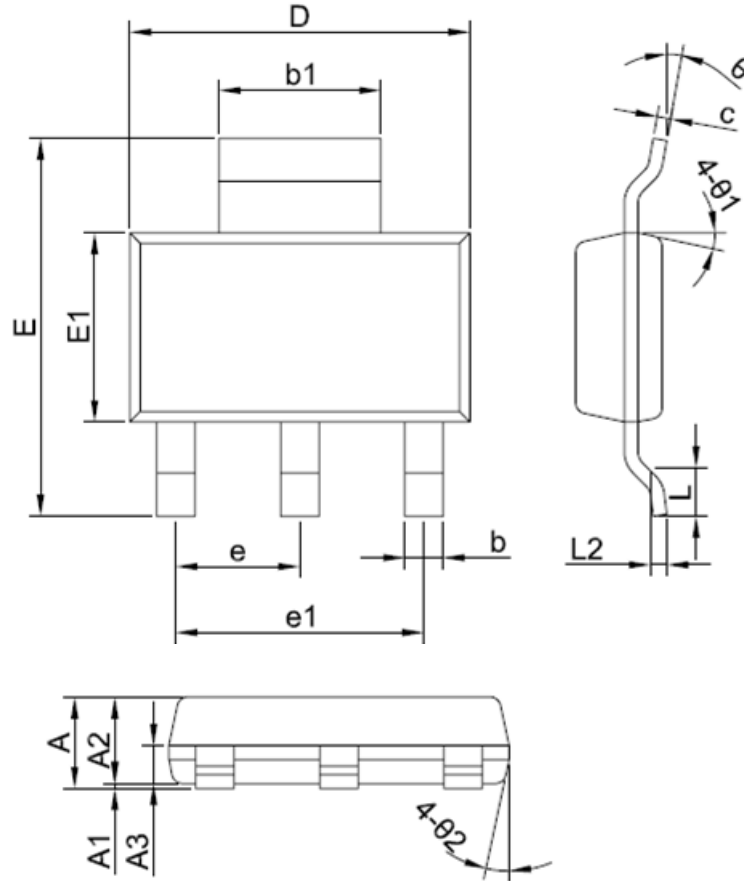
No.6 On-Resistance vs. Drain Current



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SOT-223 PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	1.52	--	1.80
A1	0.00	--	0.12
A2	1.25	1.60	1.75
A3	0.60	0.70	0.82
b	0.60	--	0.82
b1	2.90	--	3.10
c	0.24	--	0.35
D	6.20	6.30	6.50
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 REF		
e1	4.60 REF		
L	0.90MIN		
L2	0.30BSC		
theta	0°	--	10°
theta1	10°	12°	14°
theta2	10°	12°	14°



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