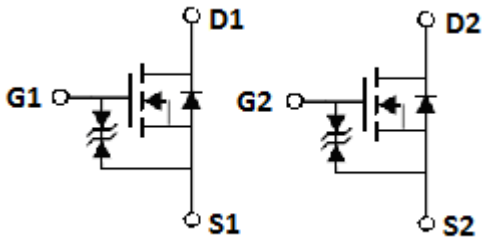
SPN8620
Dual N-Channel Enhancement Mode MOSFET

DESCRIPTION
The SPN8620 is a dual N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN8620 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

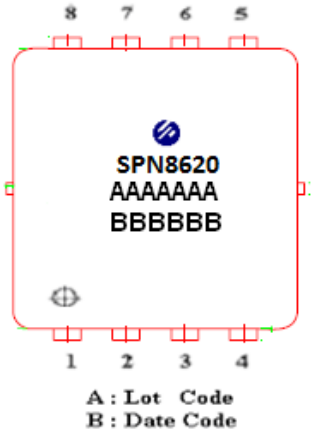
APPLICATIONS
- Powered System
- DC/DC Converter
- Load Switch

FEATURES
- 20V/4A, $R_{DS(ON)}$=12mΩ@V_{GS}=4.5V
- 20V/2A,$R_{DS(ON)}$ =14mΩ@V_{GS}=2.5V
- 20V/1.5A,$R_{DS(ON)}$=21mΩ@V_{GS}=1.8V
- High density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK3x3-8L* package design

PIN CONFIGURATION (PPAK3x3-Dual 8L)



PART MARKING



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PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source
2	G1	Gate
3	S2	Source
4	G2	Gate
5	D2	Drain
6	D2	Drain
7	D1	Drain
8	D1	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8620DN8RGB	PPAK3x3-Dual 8L	SPN8620

※ SPN8620DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate –Source Voltage		V_{GSS}	±12	V
Continuous Drain Current*	T_C=25℃	I_D	25	A
	T_C=70℃		19	
Pulsed Drain Current		I_{DM}	100	A
Power Dissipation @ T_C=25℃		P_D	26	W
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JC}$	4.8	℃/W

*Limited by the package.

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250uA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.5		1	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±10	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=16V,V_{GS}=0V			1	uA
		V_{DS}=16V,V_{GS}=0V T_J=55℃			5	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}= 4.5V,I_D=4A			12	mΩ
		V_{GS}= 2.5V,I_D=2A			14	mΩ
		V_{GS}= 1.8V,I_D=1.5A			21	mΩ
Forward Transconductance	gfs	V_{DS}=10V,I_D=5A		12		S
Gate resistance	Rg	f=1MHz		1.8		Ω
Diode Forward Voltage	V_{SD}	I_S=1A,V_{GS} =0V			1	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=10V, V_{GS}=4.5V I_D= 5A		17		nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			4		
Input Capacitance	C_{iss}	V_{DS}=10V,V_{GS}=0V f=1MHz		1020		pF
Output Capacitance	C_{oss}			160		
Reverse Transfer Capacitance	C_{rss}			110		
Turn-On Time	$t_{d(on)}$	V_{DD}=10V, I_D≡10A, V_{GEN}=10V R_G=1.5Ω		6.8		nS
	t_r			20		
Turn-Off Time	$t_{d(off)}$			42		
	t_f			13.7		

TYPICAL CHARACTERICS

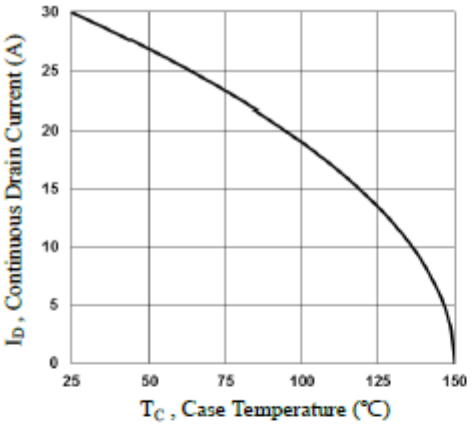

Fig.1 Continuous Drain Current vs. T_c

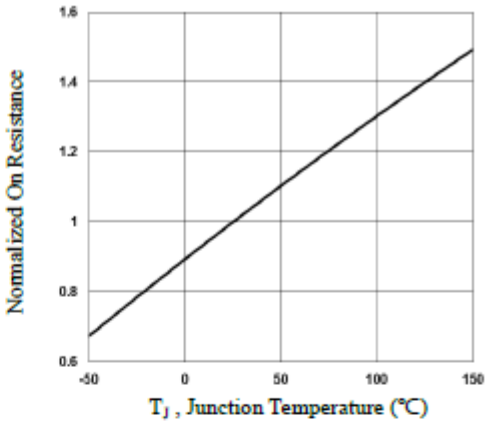

Fig.2 Normalized RDSON vs. T_J

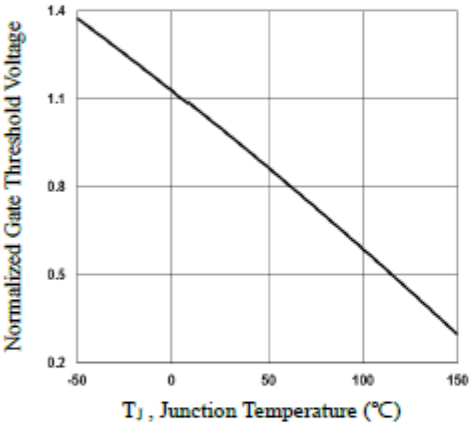

Fig.3 Normalized V_{th} vs. T_J

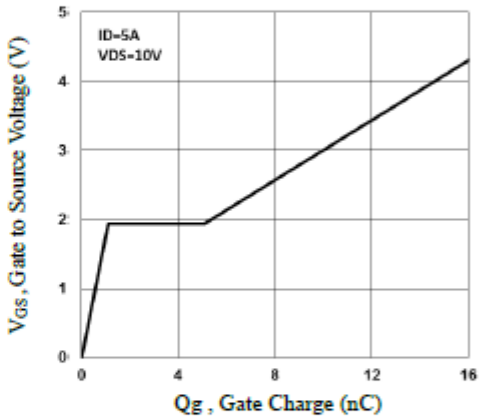

Fig.4 Gate Charge Waveform

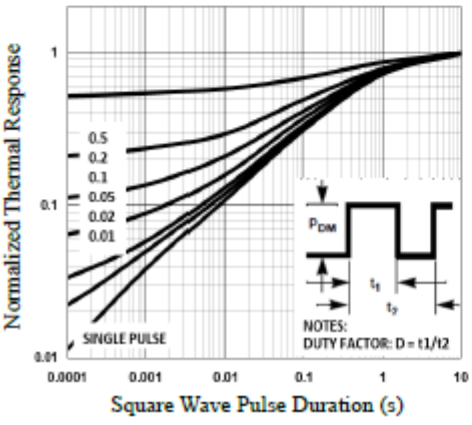

Fig.5 Normalized Transient Response

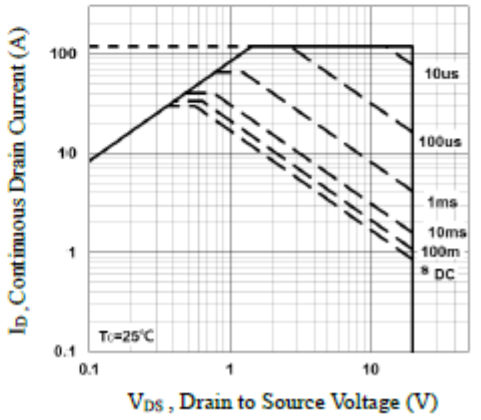

Fig.6 Maximum Safe Operation Area

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