



SPN8632

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8632 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

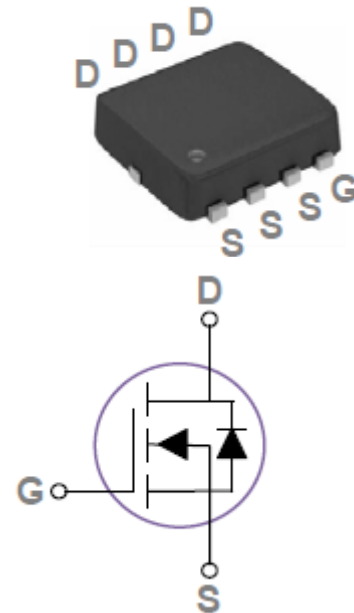
FEATURES

- ◆ 30V/96A, $R_{DS(ON)}=4.2m\Omega@V_{GS}=10V$
- ◆ 30V/96A, $R_{DS(ON)}=6m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK3x3-8L package design

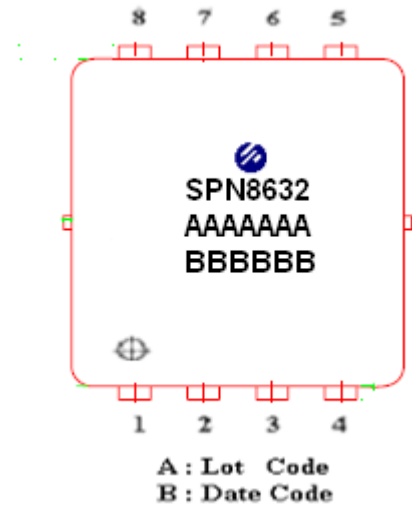
APPLICATIONS

- MB/VGA/Vcore
- POL Applications
- SMPS 2nd SR

PIN CONFIGURATION(PPAK3x3-8L)



PART MARKING





SPN8632

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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8632DN8RGB	PPAK3x3-8L	SPN8632

※ SPN8632DN8RGB : 13" Tape Reel ; Pb – Free; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	30	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current (Silicon Limited)	I _D	T _C =25°C	96	A
		T _C =100°C	68	
Pulsed Drain Current	I _{DM}	120	A	
Continuous Source Current(Diode Conduction)	I _S	30	A	
Power Dissipation	P _D	7	W	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	62	°C/W	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _{DS} =250uA	1.2	1.6	2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V, T _J =25°C			1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =125°C			10	
Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} =10V, I _D =30A		3.8	4.2	mΩ
		V _{GS} =4.5V, I _D =15A		5.2	6	
Forward Transconductance	g _{fs}	V _{DS} =10V, I _D =6A		12		S
Diode Forward Voltage	V _{SD}	I _F =1A, V _{GS} =0V			1	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V, V _{GS} =4.5V, I _D =12A		24	34	nC
Gate-Source Charge	Q _{gs}			4.2	6	
Gate-Drain Charge	Q _{gd}			13	18	
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =25V, F=1MHz		2200	3190	pF
Output Capacitance	C _{oss}			280	405	
Reverse Transfer Capacitance	C _{rss}			177	255	
Turn-On Time	t _{d(on)}	(V _{DD} =15V, I _D =15A, V _{GEN} =10V, R _G =3.3Ω)		12.6	24	nS
	t _r			19.5	37	
Turn-Off Time	t _{d(off)}			42.8	81	
	t _f			13.2	25	



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TYPICAL CHARACTERISTICS

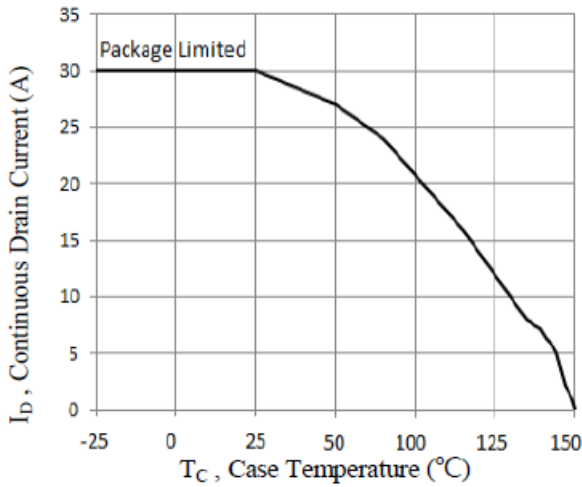


Fig.1 Continuous Drain Current vs. T_C

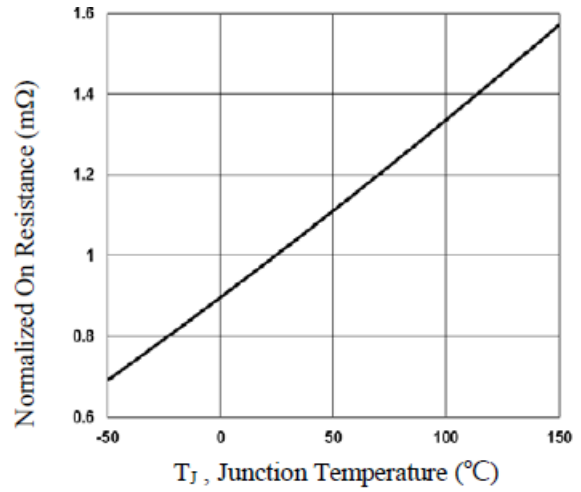


Fig.2 Normalized $R_{DS(on)}$ vs. T_J

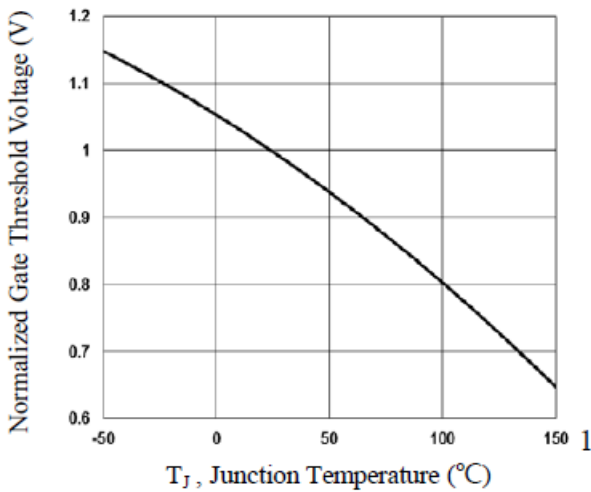


Fig.3 Normalized V_{th} vs. T_J

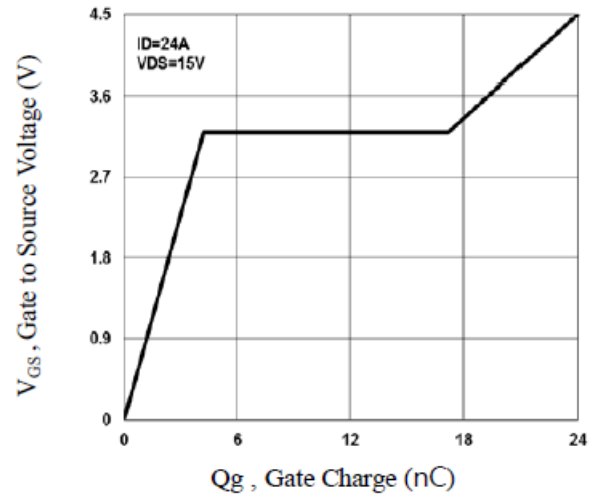


Fig.4 Gate Charge Waveform

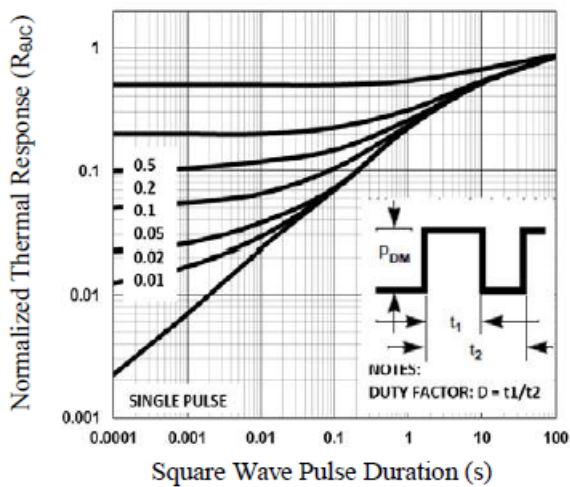


Fig.5 Normalized Transient Impedance

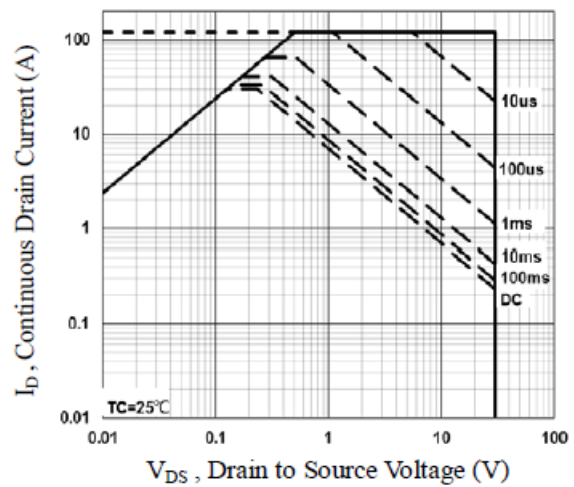


Fig.6 Maximum Safe Operation Area



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TYPICAL CHARACTERISTICS

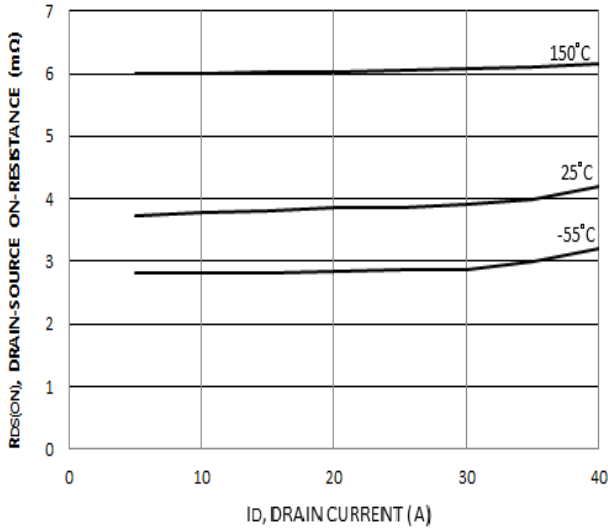


Fig.7 Typical On-Resistance vs. Drain Current and Temperature

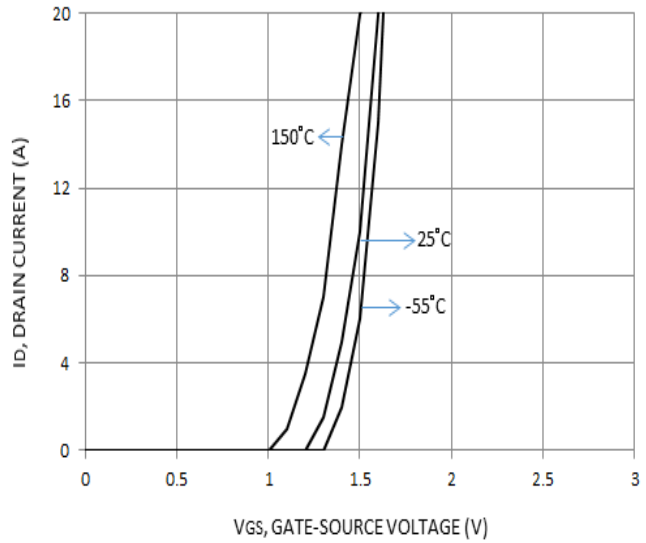
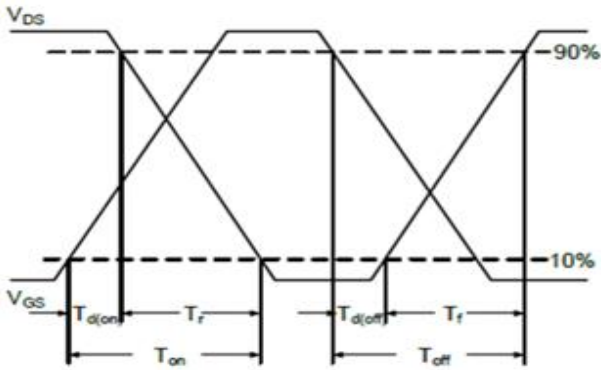
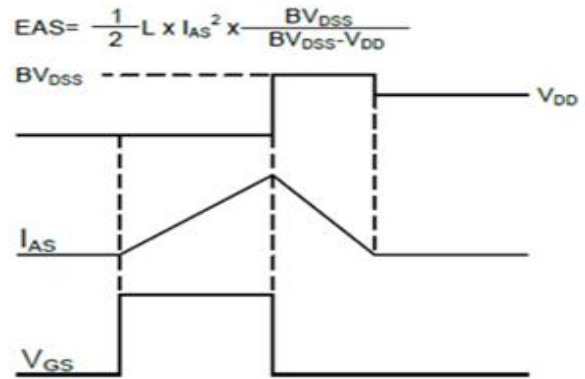


Fig.8 Typical Transfer Characteristic



Switching Time Waveform



EAS Waveform



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