



SPN8632 N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8632 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

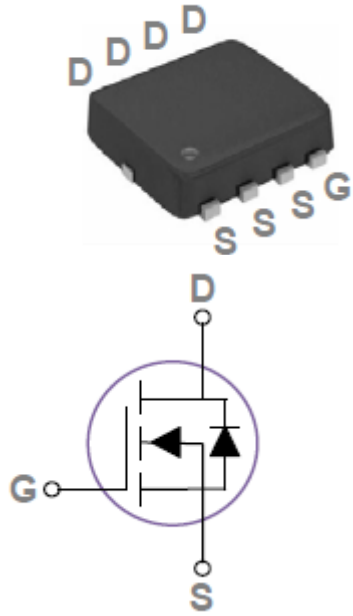
FEATURES

- ◆ 30V/30A, $R_{DS(ON)}=4.2m\Omega@V_{GS}=10V$
- ◆ 30V/15A, $R_{DS(ON)}=6m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK3x3 package design

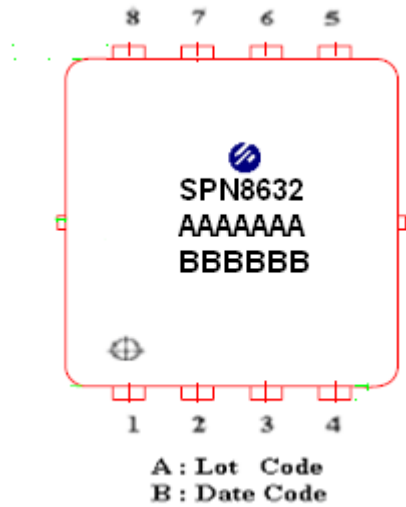
APPLICATIONS

- MB/VGA/Vcore
- POL Applications
- SMPS 2nd SR

PIN CONFIGURATION(PPAK3x3-8L)



PART MARKING





SPN8632

N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8632DN8RGB	PPAK3x3-8L	SPN8632

※ SPN8632DN8RGB : 13" Tape Reel ; Pb – Free; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	30	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	T _A =25°C	96	A
		T _A =100°C	68	
Pulsed Drain Current	I _{DM}	120	A	
Continuous Source Current(Diode Conduction)	I _S	30	A	
Power Dissipation	P _D	7	W	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	62	°C/W	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1.2	1.6	2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V,$ $T_J=25^\circ C$			1	uA
		$V_{DS}=24V, V_{GS}=0V,$ $T_J=125^\circ C$			10	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=30A$		3.8	4.2	mΩ
		$V_{GS}=4.5V, I_D=15A$		5.2	6	
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=6A$		12		S
Diode Forward Voltage	V_{SD}	$I_F=1A, V_{GS}=0V$			1	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=4.5V,$ $I_D=12A$		24	34	nC
Gate-Source Charge	Q_{gs}			4.2	6	
Gate-Drain Charge	Q_{gd}			13	18	
Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $F=1MHz$		2200	3190	pF
Output Capacitance	C_{oss}			280	405	
Reverse Transfer Capacitance	C_{rss}			177	255	
Turn-On Time	$t_{d(on)}$	$(V_{DD}=15V, I_D=15A,$ $V_{GEN}=10V, R_G=3.3\Omega)$		12.6	24	ns
	t_r			19.5	37	
Turn-Off Time	$t_{d(off)}$			42.8	81	
	t_f			13.2	25	



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TYPICAL CHARACTERISTICS

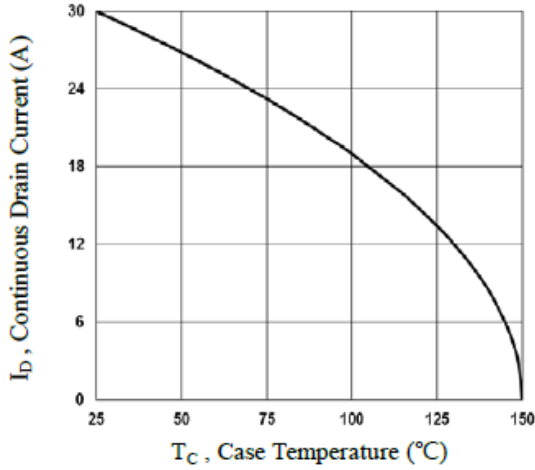


Fig.1 Continuous Drain Current vs. T_C

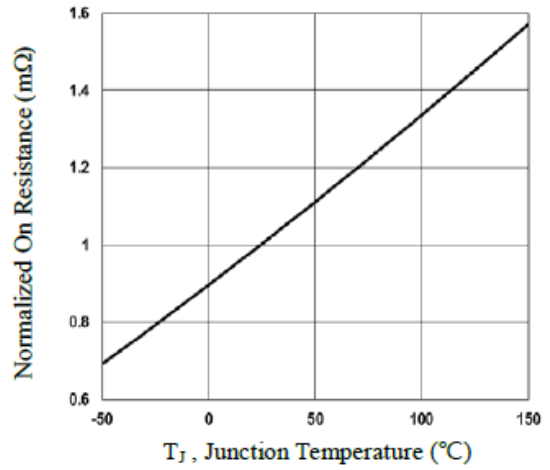


Fig.2 Normalized $R_{DS(on)}$ vs. T_J

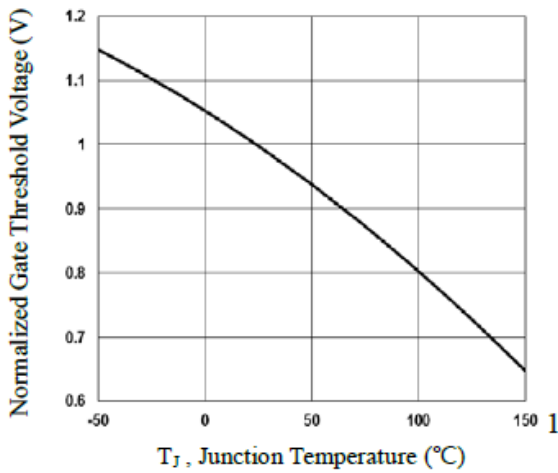


Fig.3 Normalized V_{th} vs. T_J

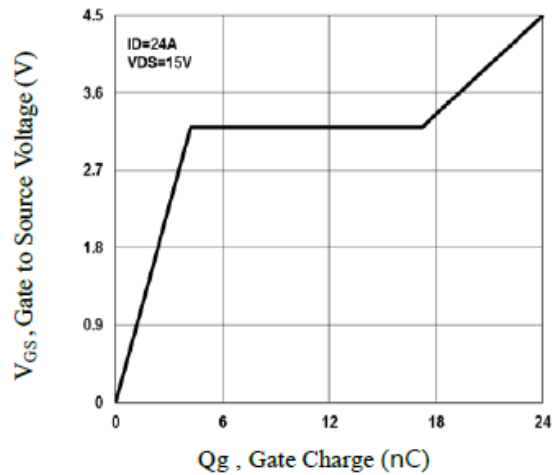


Fig.4 Gate Charge Waveform

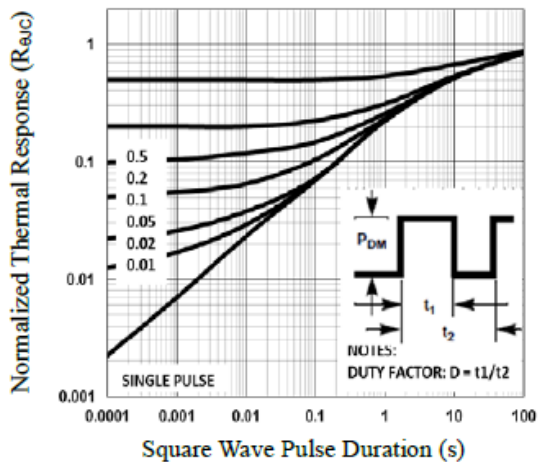


Fig.5 Normalized Transient Impedance

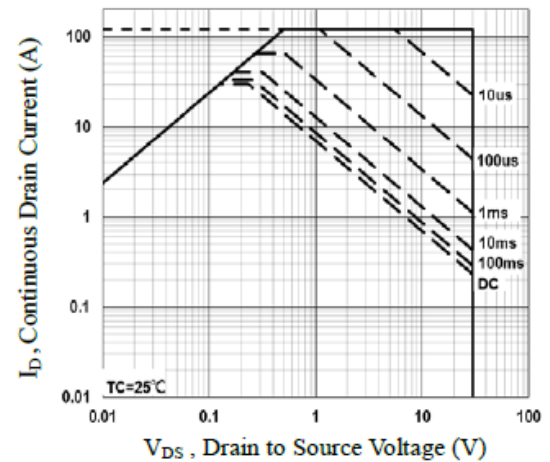


Fig.6 Maximum Safe Operation Area



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TYPICAL CHARACTERISTICS

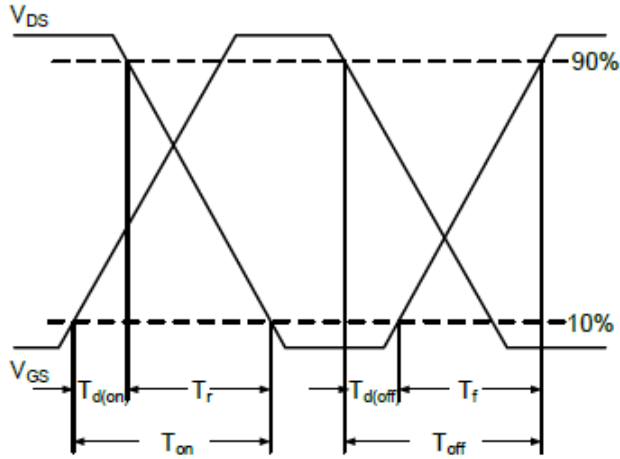


Fig.7 Switching Time Waveform

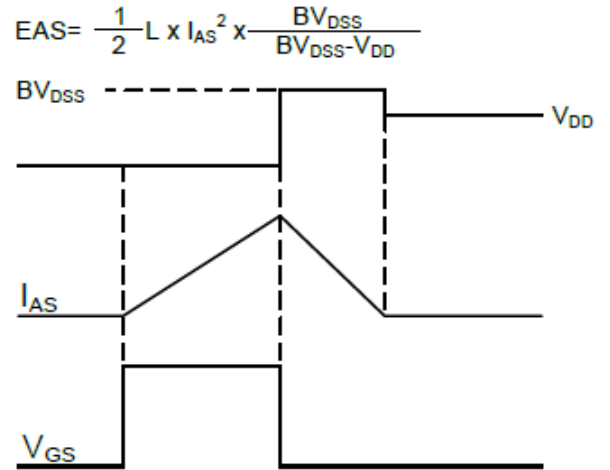
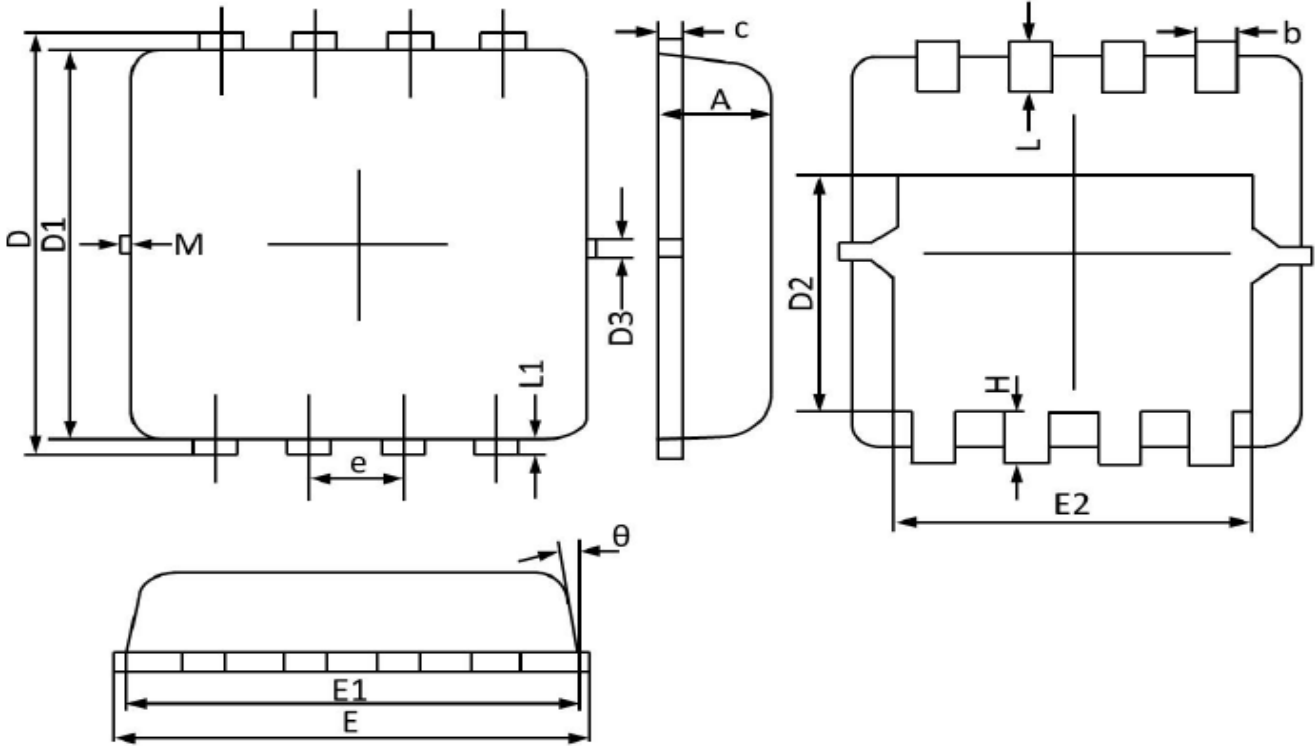


Fig.8 EAS Waveform



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PPAK3x3-8L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.013
c	0.100	0.250	0.004	0.009
D	3.250	3.450	0.128	0.135
D1	3.000	3.200	0.119	0.125
D2	1.780	1.980	0.070	0.077
D3	0.130 REF		0.005 REF	
E	3.200	3.400	0.126	0.133
E1	3.000	3.200	0.119	0.125
E2	2.390	2.590	0.094	0.102
e	0.650 BSC		0.026 BSC	
H	0.300	0.500	0.011	0.019
L	0.300	0.500	0.011	0.019
L1	0.130 REF		0.005 REF	
theta	0°	12°	0°	12°
M	0.150 REF		0.006 REF	



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