



SPN8668 N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8668 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high efficiency and fast switching is required.

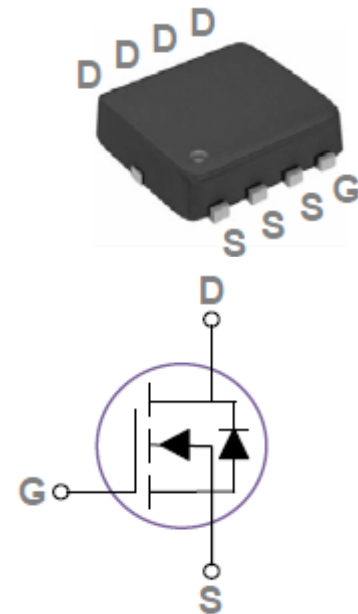
FEATURES

- ◆ 60V/33A, $R_{DS(ON)}=21m\Omega@V_{GS}=10V$
- ◆ 60V/8A, $R_{DS(ON)}=24m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK3x3 package design

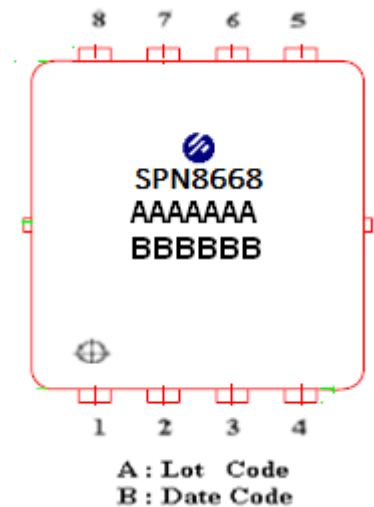
APPLICATIONS

- Motor Drive
- Power Tools
- LED Lighting

PIN CONFIGURATION(PPAK3x3-8L)



PART MARKING





SPN8668

N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8668DN8RGB	PPAK3x3-8L	SPN8668

※ SPN8668DN8RGB : 13" Tape Reel ; Pb – Free; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	60	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	T _C =25°C	12	A
		T _C =100°C	8.5	
Pulsed Drain Current	I _{DM}	132	A	
Continuous Source Current(Diode Conduction)	I _S	33	A	
Power Dissipation	P _D	7	W	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	62	°C/W	
Thermal Resistance-Junction to Case	R _{θJC}	2.8	°C/W	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _{DS} =25uA	1.2	1.8	2.2	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V, T _J =25°C			1	uA
		V _{DS} =48V, V _{GS} =0V, T _J =125°C			10	
Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} =10V, I _D =15A		17	21	mΩ
		V _{GS} =4.5V, I _D =8A		20	24	
Forward Transconductance	g _{fs}	V _{DS} =10V, I _D =10A		9		S
Diode Forward Voltage	V _{SD}	I _F =1A, V _{GS} =0V			1	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =30V, V _{GS} =10V, I _D =15A		28	42	nC
Gate-Source Charge	Q _{gs}			3.5	7	
Gate-Drain Charge	Q _{gd}			6.5	10	
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =20V, F=1MHz		1680	2440	pF
Output Capacitance	C _{oss}			115	170	
Reverse Transfer Capacitance	C _{rss}			85	125	
Turn-On Time	t _{d(on)}	(V _{DD} =30V, I _D =-1A, V _{GEN} =10V, R _G =6Ω)		7.2	14	ns
	t _r			38	72	
Turn-Off Time	t _{d(off)}			34	65	
	t _f			8.2	16	



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TYPICAL CHARACTERISTICS

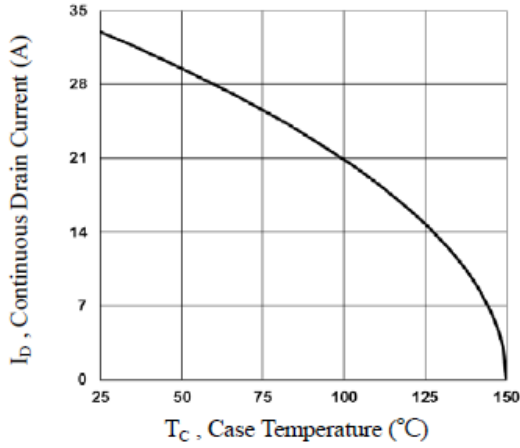


Fig.1 Continuous Drain Current vs. T_C

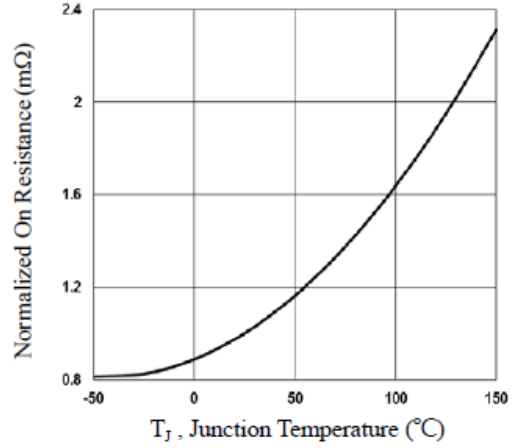


Fig.2 Normalized R_{DSON} vs. T_J

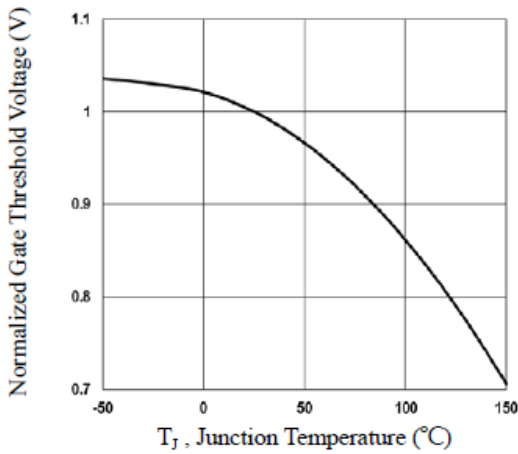


Fig.3 Normalized V_{th} vs. T_J

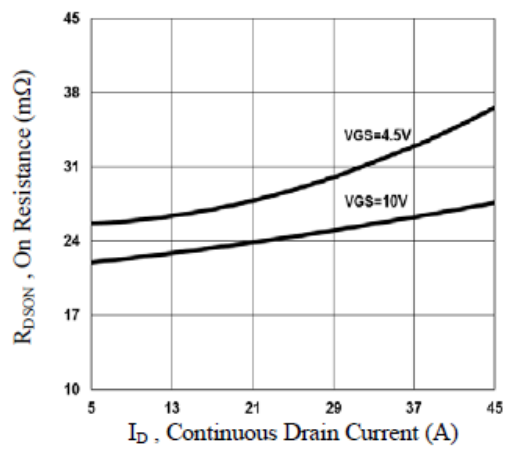


Fig.4 R_{DSON} vs. Continuous Drain Current

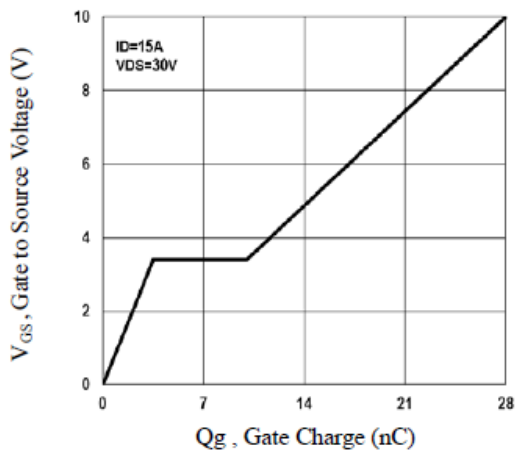


Fig.5 Gate Charge Waveform

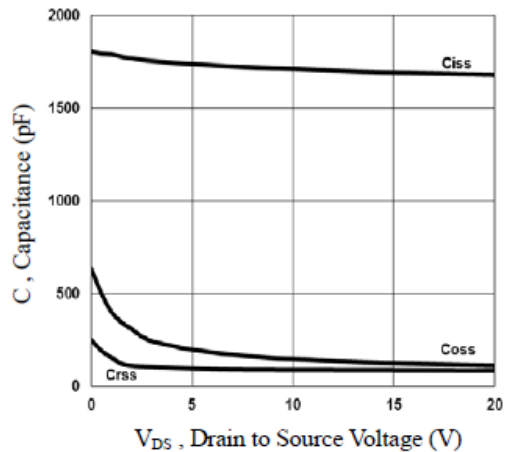


Fig.6 Capacitance Characteristics



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TYPICAL CHARACTERISTICS

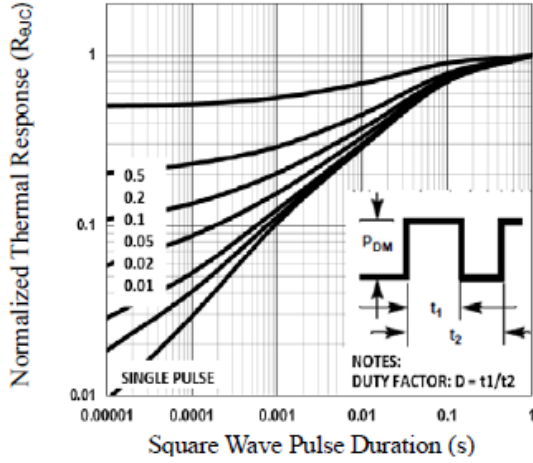


Fig.7 Normalized Transient Impedance

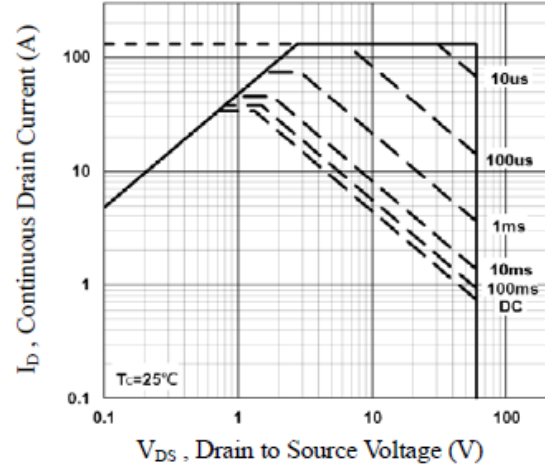


Fig.8 Maximum Safe Operation Area

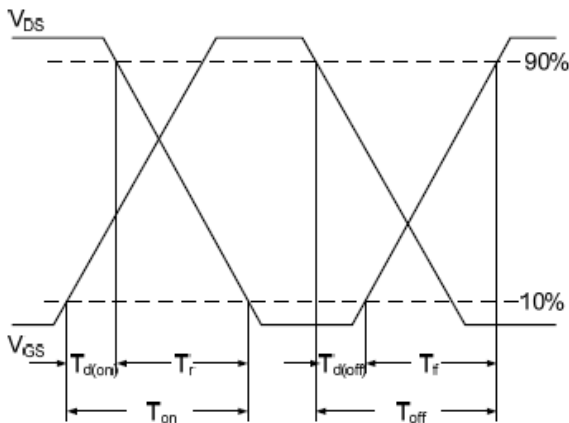


Fig.9 Switching Time Waveform

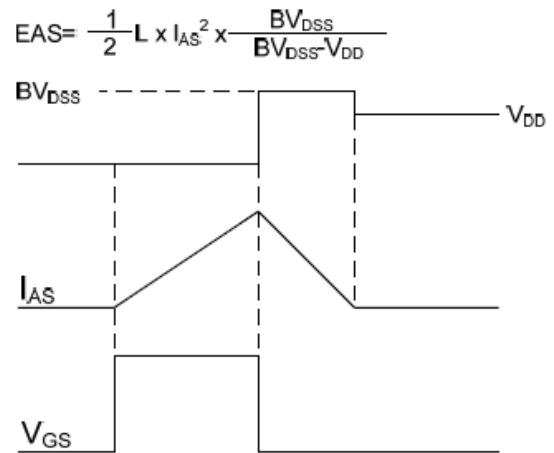


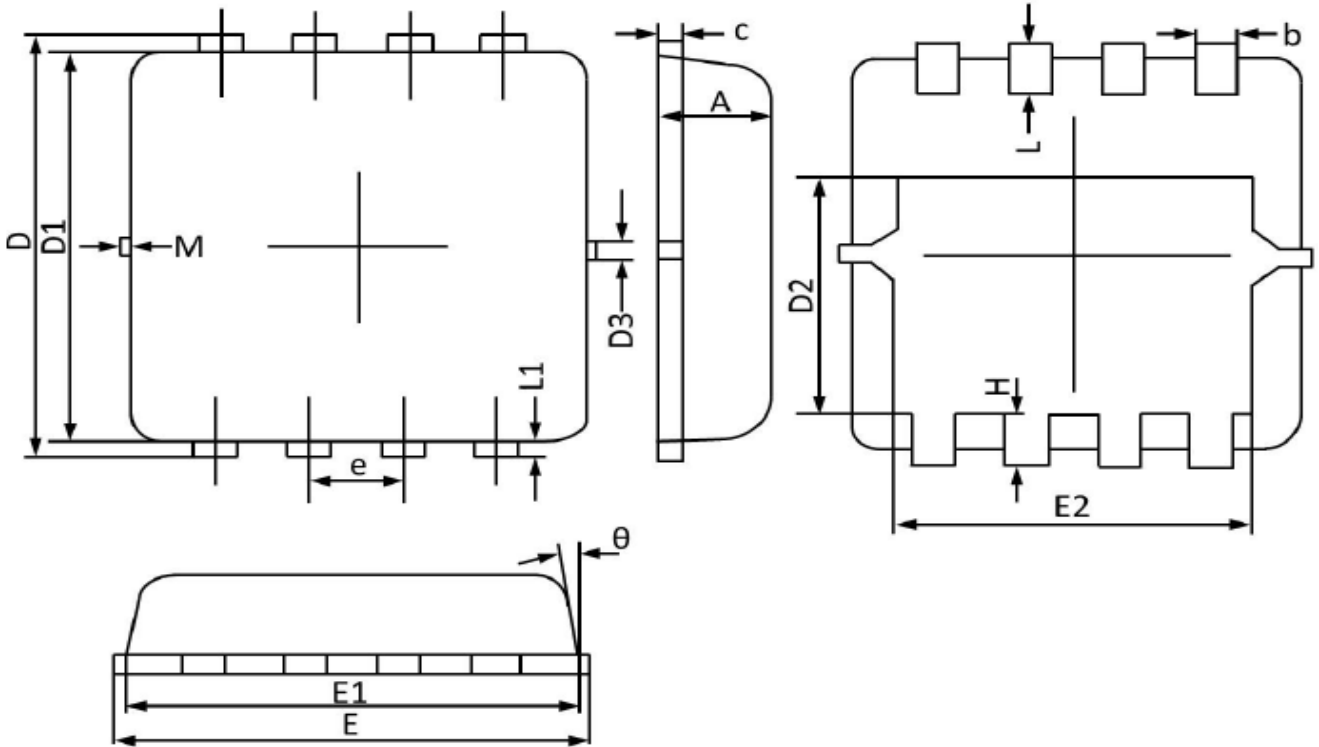
Fig.10 EAS Waveform



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PPAK3x3-8L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.013
c	0.100	0.250	0.004	0.009
D	3.250	3.450	0.128	0.135
D1	3.000	3.200	0.119	0.125
D2	1.780	1.980	0.070	0.077
D3	0.130 REF		0.005 REF	
E	3.200	3.400	0.126	0.133
E1	3.000	3.200	0.119	0.125
E2	2.390	2.590	0.094	0.102
e	0.650 BSC		0.026 BSC	
H	0.300	0.500	0.011	0.019
L	0.300	0.500	0.011	0.019
L1	0.130 REF		0.005 REF	
theta	0°	12°	0°	12°
M	0.150 REF		0.006 REF	



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