



# SPN8668 N-Channel Enhancement Mode MOSFET

## DESCRIPTION

The SPN8668 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high efficiency and fast switching is required.

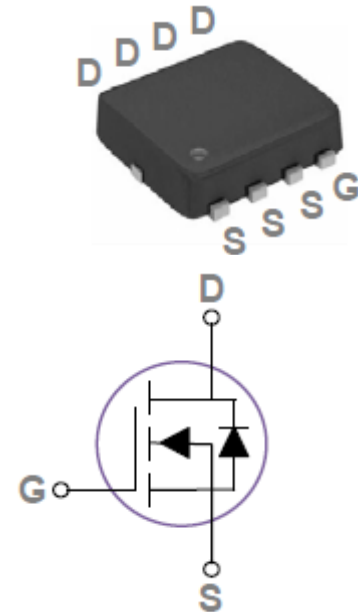
## FEATURES

- ◆ 60V/80A,  $R_{DS(ON)}=21m\Omega@V_{GS}=10V$
- ◆ 60V/80A,  $R_{DS(ON)}=24m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK3x3-8L package design

## APPLICATIONS

- Motor Drive
- Power Tools
- LED Lighting

## PIN CONFIGURATION(PPAK3x3-8L)



## PART MARKING





# SPN8668

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### PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8668DN8RGB	PPAK3x3-8L	SPN8668

※ SPN8668DN8RGB : 13" Tape Reel ; Pb – Free; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	60	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>C</sub> =25°C	80	A
		T <sub>C</sub> =100°C	57	
Pulsed Drain Current	I <sub>DM</sub>	132	A	
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	33	A	
Power Dissipation	P <sub>D</sub>	7	W	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	62	°C/W	
Thermal Resistance-Junction to Case	R <sub>θJC</sub>	2.8	°C/W	



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### ELECTRICAL CHARACTERISTICS

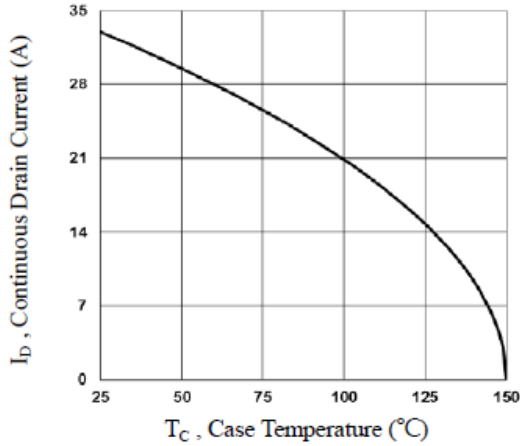
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_{DS}=25\mu A$	1.2	1.8	2.2	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V, T_J=25^\circ C$			1	uA
		$V_{DS}=48V, V_{GS}=0V, T_J=125^\circ C$			10	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=15A$		17	21	mΩ
		$V_{GS}=4.5V, I_D=8A$		20	24	
Forward Transconductance	$g_{fs}$	$V_{DS}=10V, I_D=10A$		9		S
Diode Forward Voltage	$V_{SD}$	$I_F=1A, V_{GS}=0V$			1	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=30V, V_{GS}=10V, I_D=15A$		28	42	nC
Gate-Source Charge	$Q_{gs}$			3.5	7	
Gate-Drain Charge	$Q_{gd}$			6.5	10	
Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=20V, F=1MHz$		1680	2440	pF
Output Capacitance	$C_{oss}$			115	170	
Reverse Transfer Capacitance	$C_{rss}$			85	125	
Turn-On Time	$t_{d(on)}$	$(V_{DD}=30V, I_D=-1A, V_{GEN}=10V, R_G=6\Omega)$		7.2	14	nS
	$t_r$			38	72	
Turn-Off Time	$t_{d(off)}$			34	65	
	$t_f$			8.2	16	

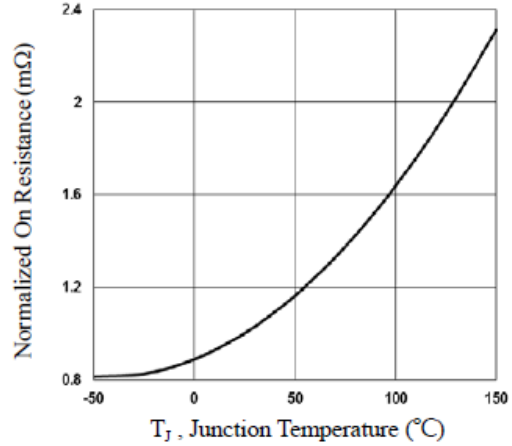


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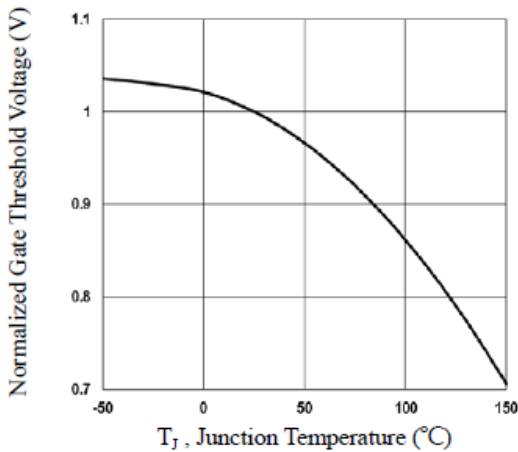
## TYPICAL CHARACTERISTICS



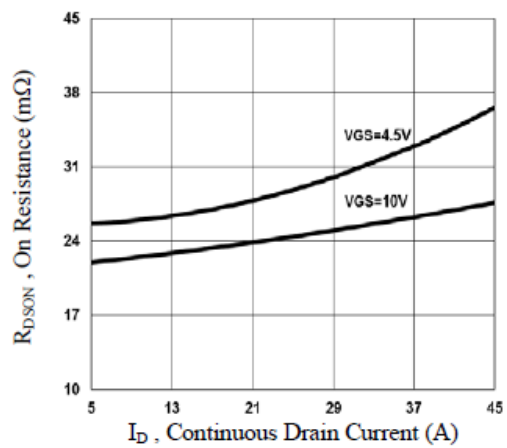
**Fig.1 Continuous Drain Current vs.  $T_C$**



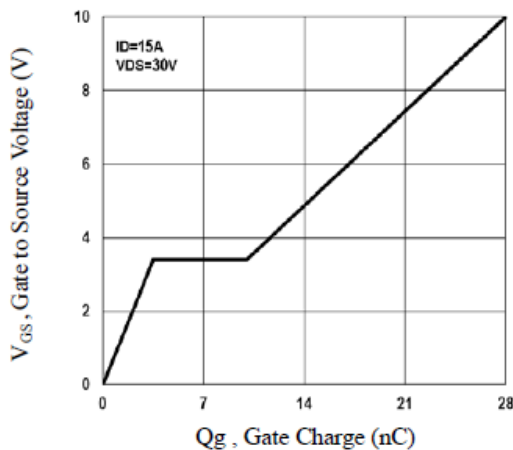
**Fig.2 Normalized  $R_{DS(on)}$  vs.  $T_J$**



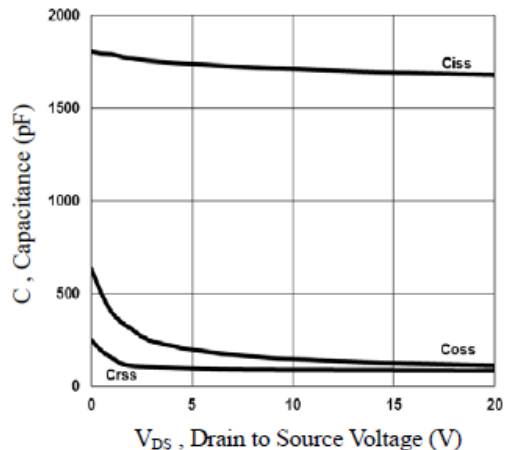
**Fig.3 Normalized  $V_{th}$  vs.  $T_J$**



**Fig.4  $R_{DS(on)}$  vs. Continuous Drain Current**



**Fig.5 Gate Charge Waveform**

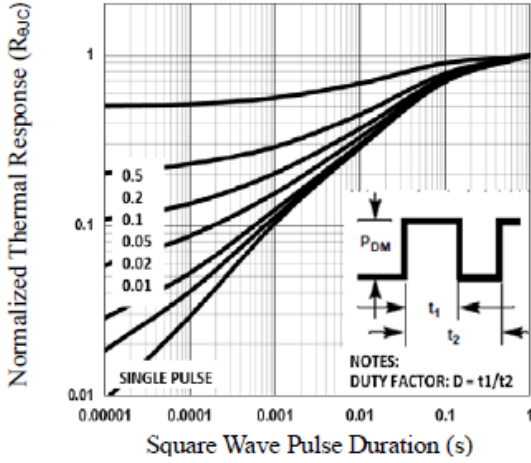


**Fig.6 Capacitance Characteristics**

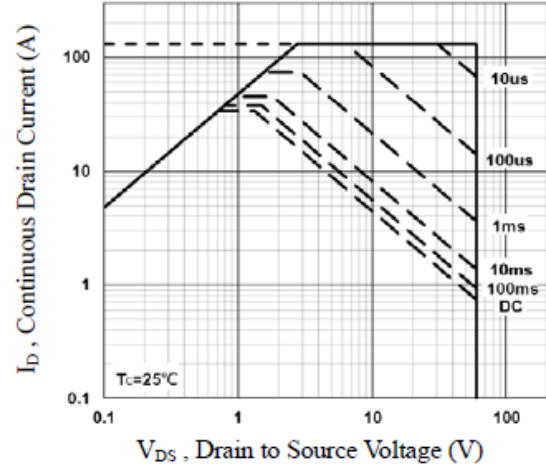


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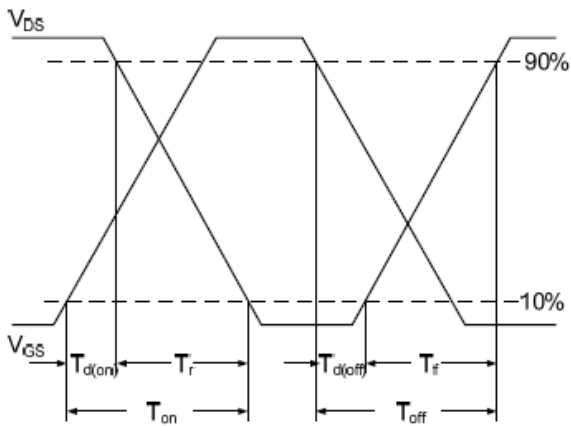
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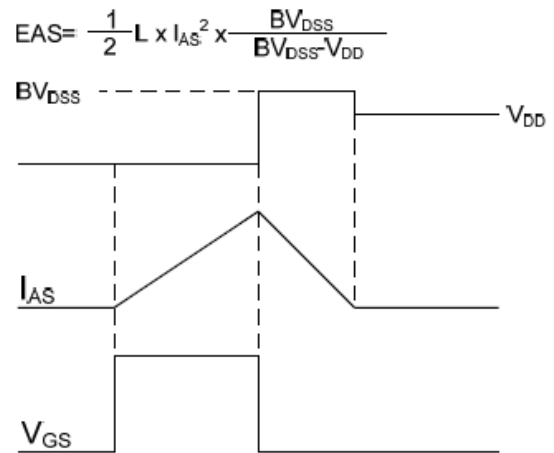
**Fig.7 Normalized Transient Impedance**



**Fig.8 Maximum Safe Operation Area**



**Fig.9 Switching Time Waveform**



**Fig.10 EAS Waveform**



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