



# SPN8812

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN8812 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN8812 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

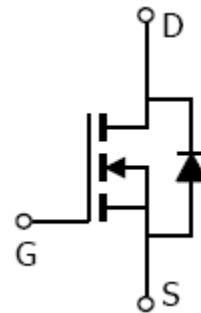
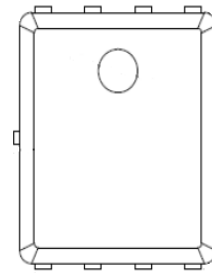
### APPLICATIONS

- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

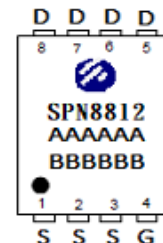
### FEATURES

- ◆ 100V/63A,  $R_{DS(ON)}=9.8m\Omega@V_{GS}=10V$
- ◆ 100V/63A,  $R_{DS(ON)}=13.0m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK5x6-8L package design

### PIN CONFIGURATION(PPAK5x6-8L)



### PART MARKING



A : Lot Code  
 B : Date Code  
 (YY/MM/DD)



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### PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8812DN8RGB	PPAK5x6-8L	SPN8812

※ SPN8812DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	100	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current (Silicon Limited)	I <sub>D</sub>	T <sub>C</sub> =25°C	63	A
		T <sub>C</sub> =100°C	40	
Pulsed Drain Current	I <sub>DM</sub>	160	A	
Single Pulse Avalanche Energy ( T <sub>C</sub> =25°C , L=0.1mH. )	E <sub>AS</sub>	31	mJ	
Power Dissipation (T <sub>C</sub> =25°C)	P <sub>D</sub>	83	W	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Case	R <sub>θJC</sub>	1.5	°C/W	



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### ELECTRICAL CHARACTERISTICS

(TA=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.4	1.8	2.4	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$			1	uA
		$V_{DS}=80V, V_{GS}=0V, T_J=85^\circ C$			10	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		8	9.8	mΩ
		$V_{GS}=4.5V, I_D=20A$		10.5	13	
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=10A$		80		S
Gate resistance	$R_g$	$V_{DS}=0V, V_{GS}=0V$ $f=1MHz$		1.4		Ω
<b>Dynamic</b>						
Total Gate Charge	$Q_g(10V)$	$V_{DS}=50V, V_{GS}=10V$ $I_D=20A$		24		nC
Total Gate Charge	$Q_g(4.5V)$			12		
Gate-Source Charge	$Q_{gs}$			4		
Gate-Drain Charge	$Q_{gd}$			6		
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V$ $f=1MHz$		1450		pF
Output Capacitance	$C_{oss}$			273		
Reverse Transfer Capacitance	$C_{rss}$			5		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V,$ $I_D=20A, V_{GS}=10V$ $R_G=10\Omega$		6		nS
	$t_r$			4		
Turn-Off Time	$t_{d(off)}$			18		
	$t_f$			3		
<b>Reverse Diodes</b>						
Diode Forward Voltage	$V_{SD}$	$I_S=20A, V_{GS}=0V$		0.9	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_R=50V, I_F=20A,$		40		nS
Reverse Recovery Charge	$Q_{rr}$	$dI_F/dt=500A/\mu S$		162		nC



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## TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

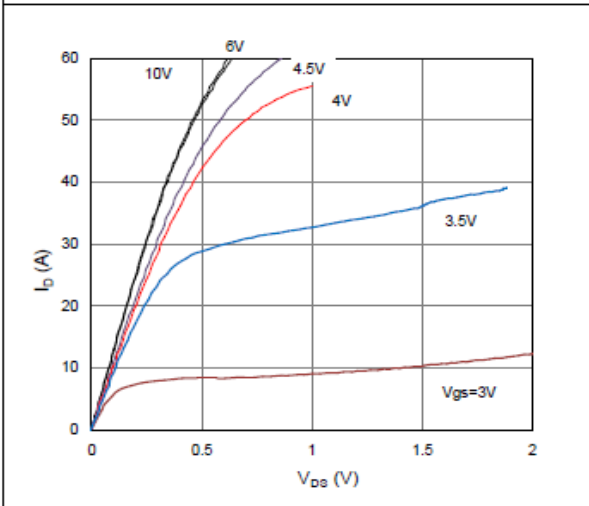


Figure 2. On-Resistance vs. Gate-Source Voltage

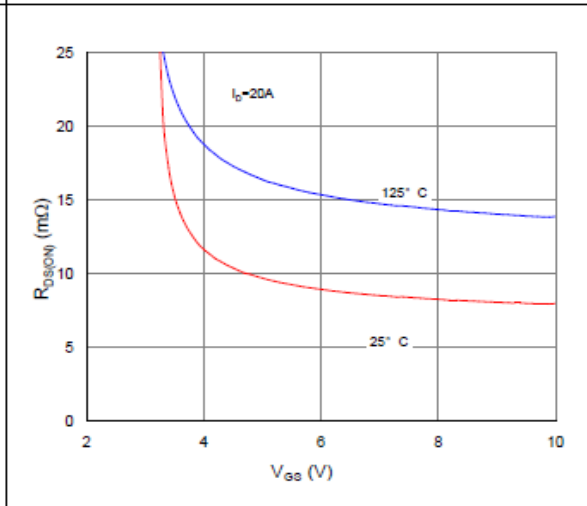


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

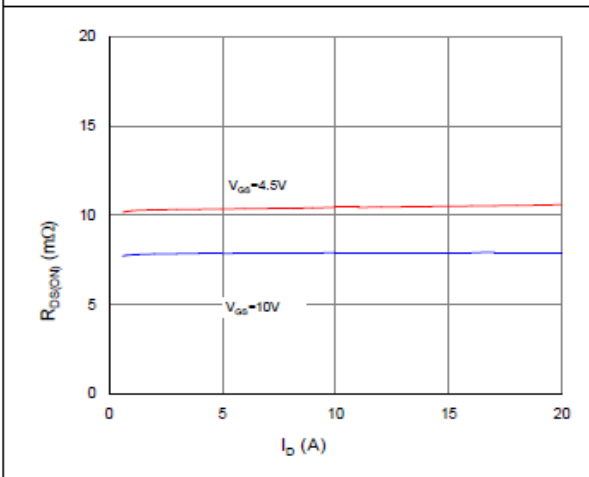


Figure 4. Normalized On-Resistance vs. Junction Temperature

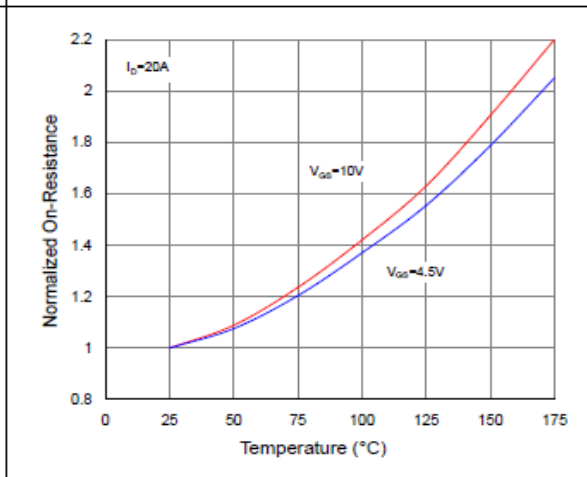


Figure 5. Typical Transfer Characteristics

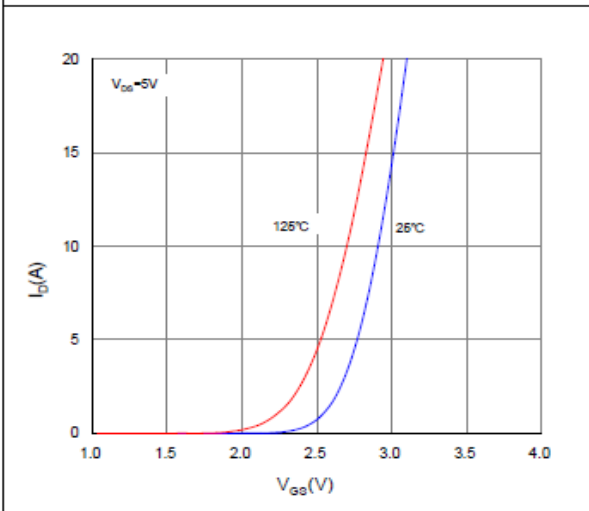
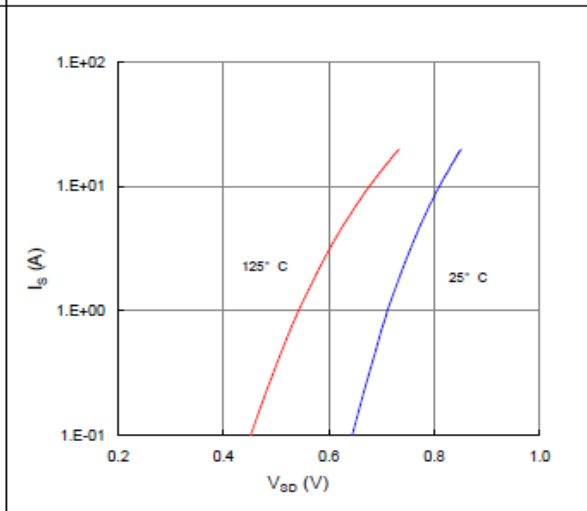


Figure 6. Typical Source-Drain Diode Forward Voltage





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## TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

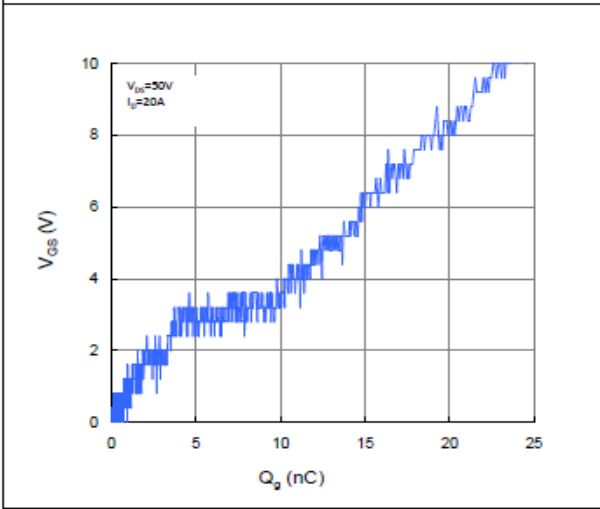


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

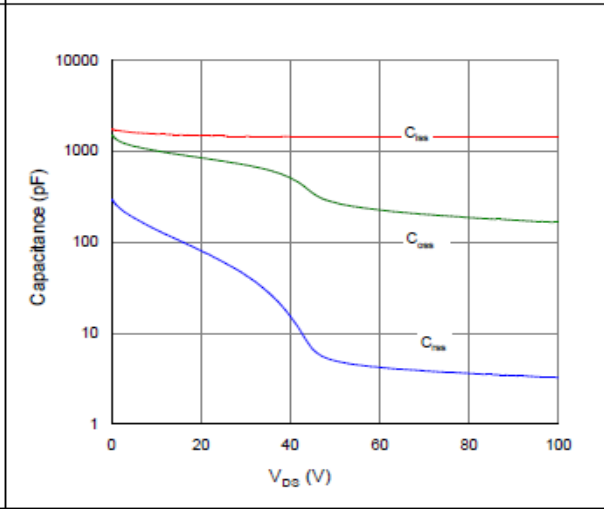


Figure 9. Maximum Safe Operating Area

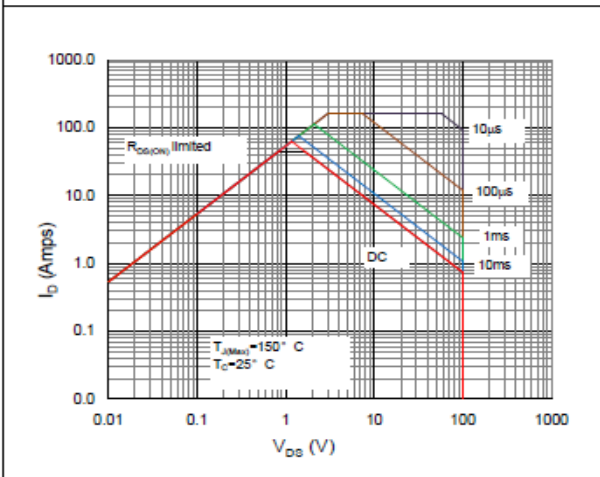


Figure 10. Maximum Drain Current vs. Case Temperature

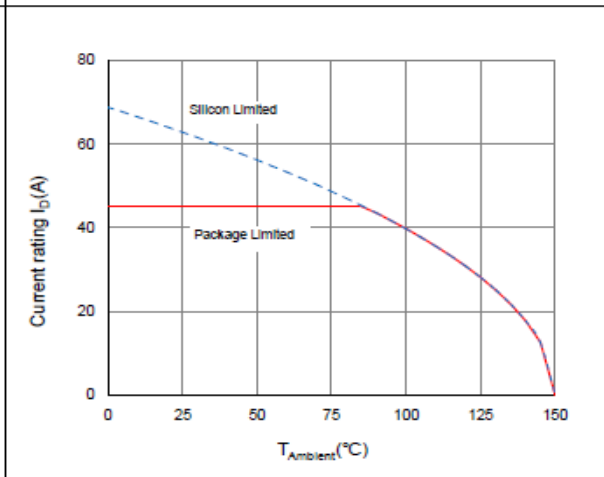
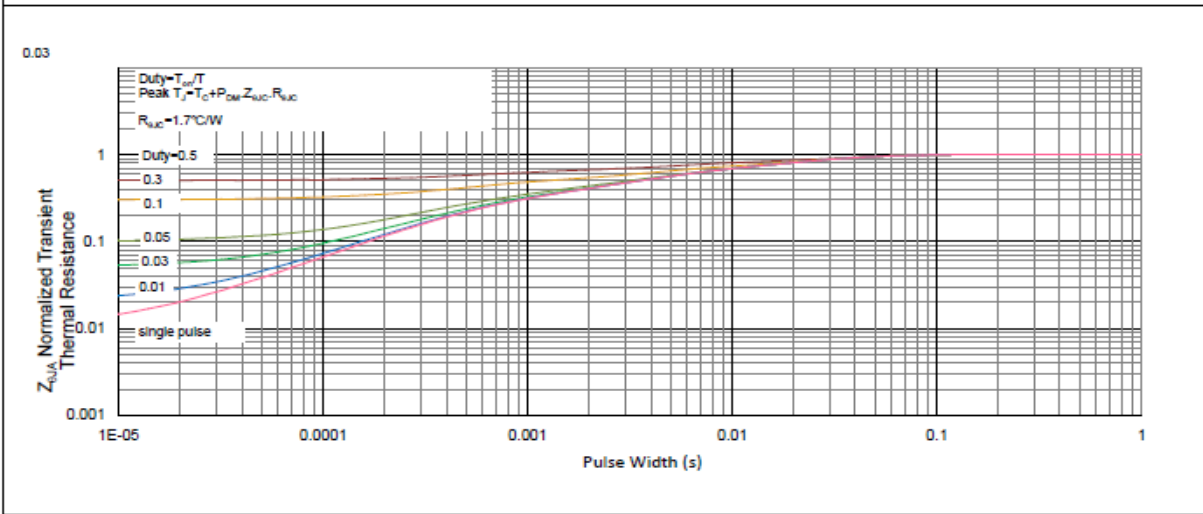


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





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