



SPN8860 N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8860 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for most of synchronous buck converter applications.

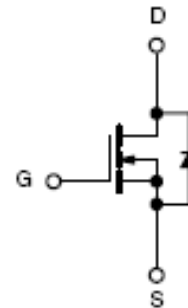
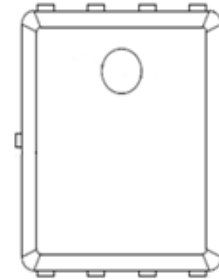
APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter

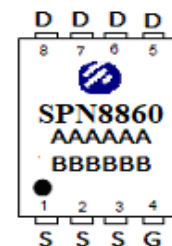
FEATURES

- ◆ 60V/20A, $R_{DS(ON)}=16m\Omega@V_{GS}=10V$
- ◆ 60V/20A, $R_{DS(ON)}=19m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK5x6-8L package design

PIN CONFIGURATION (PPAK5x6-8L)



PART MARKING



A : Lot Code
 B : Date Code
 (YY / MM / DD)



SPN8860

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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8860DN8RGB	PPAK5x6-8L	SPN8860

※ SPN8860DN8RGB: Tape Reel ; Pb – Free; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	60	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	46	A
		TA=100°C	33	
Pulsed Drain Current	I _{DM}	203	A	
Avalanche Current	I _{AS}	27	A	
Power Dissipation	P _D	71	W	
Avalanche Energy with Single Pulse (T _J =25°C, L= 0.1mH, I _{AS} = 38A)	E _{AS}	36	mJ	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Case	R _{θJC}	2.1	°C/W	



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ELECTRICAL CHARACTERISTICS

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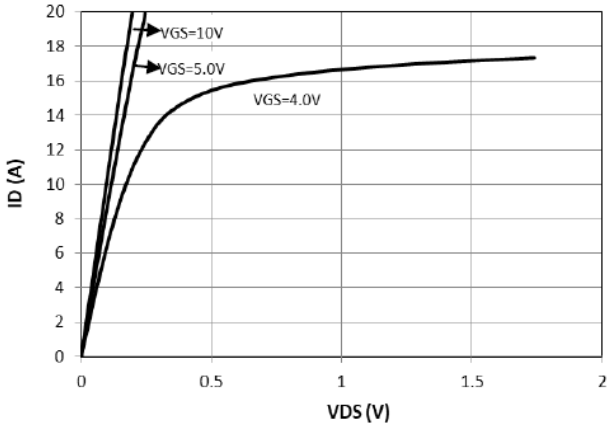
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=48V, V_{GS}=0V$			1	uA
		$V_{DS}=48V, V_{GS}=0V$ $T_J=150^\circ C$			100	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		13	16	mΩ
		$V_{GS}=4.5V, I_D=20A$		16	19	
Gate Resistance	R_G			1.3		Ω
Forward Transconductance	g_{fs}	$V_{DS}=15V, I_D=20A$		15		S
Diode Forward Voltage	V_{SD}	$I_S=40A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	$Q_{g(10V)}$	$V_{DS}=48V, V_{GS}=10V$ $I_D=40A$		29		nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			8		
Total Gate Charge	$Q_{g(4.5V)}$	$V_{DS}=48V, V_{GS}=4.5V$ $I_D=40A$		15		
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1MHz$		1400		pF
Output Capacitance	C_{oss}			137		
Reverse Transfer Capacitance	C_{rss}			95		
Turn-On Time	$t_{d(on)}$	$V_{DD}=48V, I_D=40A,$ $V_{GEN}=10V, R_G=2.5\Omega$		8.4		nS
	t_r			12.4		
Turn-Off Time	$t_{d(off)}$			26		
	t_f			4.4		



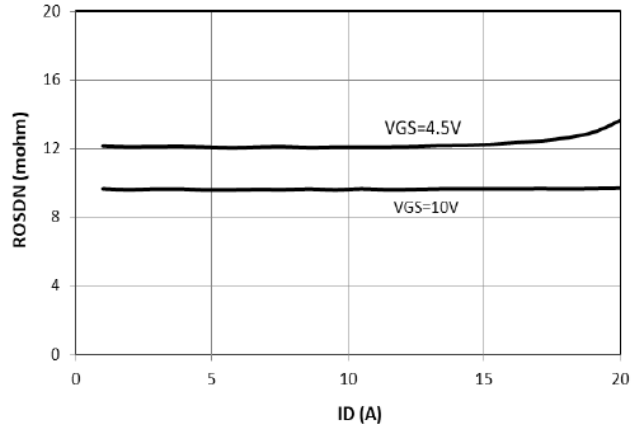
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TYPICAL CHARACTERISTICS

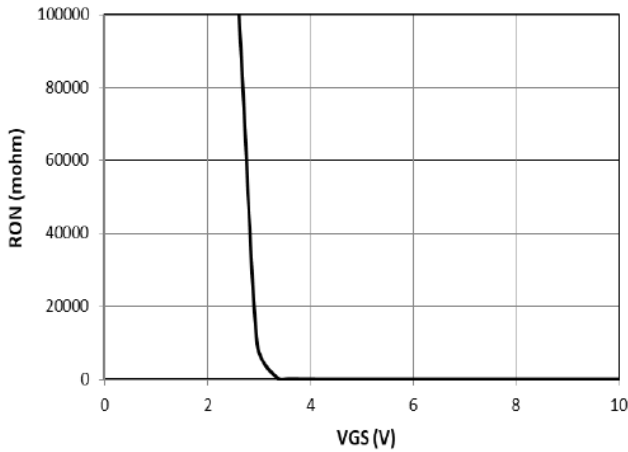
TYPICAL OUTPUT CHARACTERISTICS



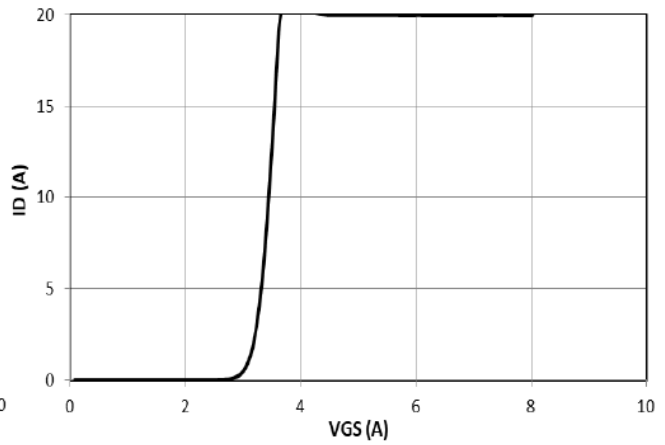
ON-RESISTANCE VS. DRAIN CURRENT AND GATE VOLTAGE



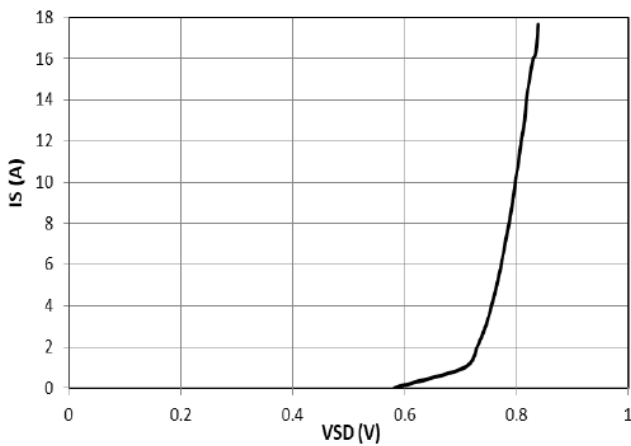
ON-RESISTANCE VS. GATE-SOURCE VOLTAGE



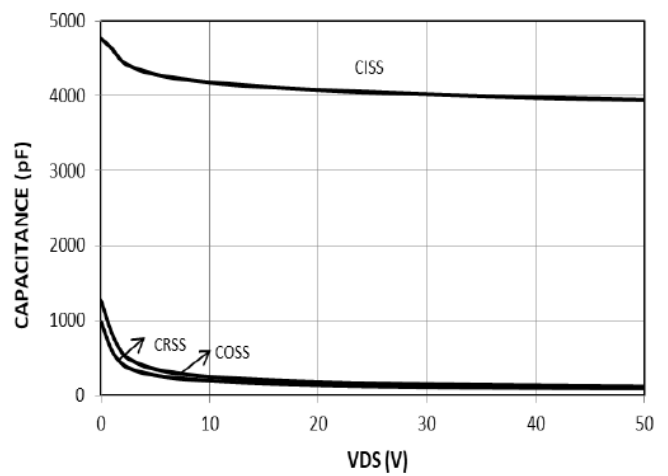
TYPICAL TRANSFER CHARACTERISTICS



TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE



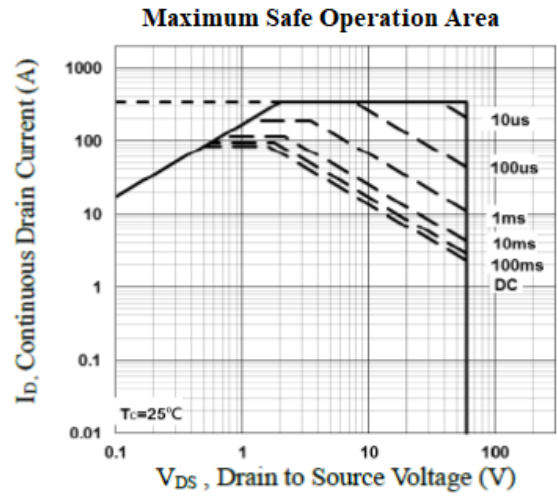
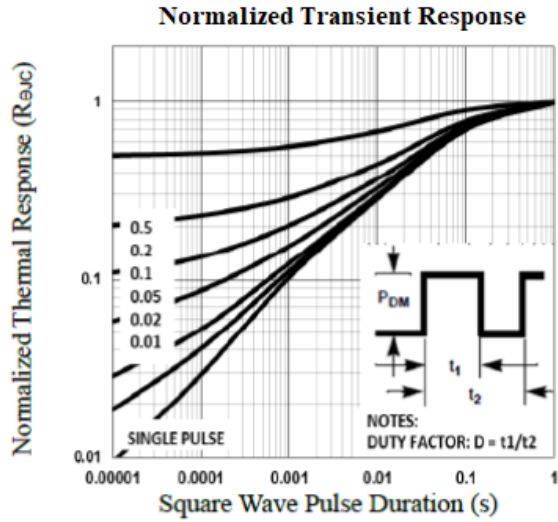
TYPICAL CAPACITANCE VS. DRAIN-SOURCE VOLTAGE





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TYPICAL CHARACTERISTICS





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