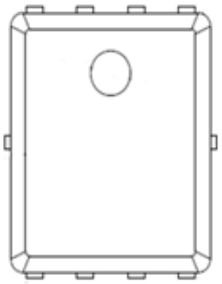
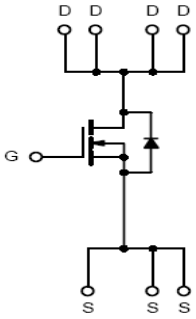
SPN8862
N-Channel Enhancement Mode MOSFET

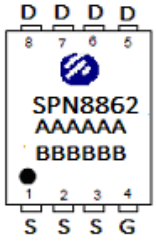
DESCRIPTION
The SPN8862 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching is required.

APPLICATIONS
- DC/DC Converter
- Load Switch
- Synchronous Buck Converter

FEATURES
- 60V/15A,$R_{DS(ON)}$=12mΩ@V_{GS}=10V
- 60V/10A,$R_{DS(ON)}$=15mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK5x6-8L package design

PIN CONFIGURATION (PPAK5x6-8L)




PART MARKING


A : Lot Code
B : Date Code
(YY / MM / DD)

SPN8862
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8862DN8RGB	PPAK5x6-8L	SPN8862

※ SPN8862DN8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_C=25℃	I_D	60	A
	T_C=70℃		38	
Pulsed Drain Current		I_{DM}	230	A
Avalanche Current		I_{AS}	38	A
Power Dissipation	T_C=25℃	P_D	83	W
	T_A=70℃		1.6	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case		$R_{\theta JC}$	1.5	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0		2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=48V,V_{GS}=0V			1	uA
		V_{DS}=48V,V_{GS}=0V T_J=55℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥5V,V_{GS} =10V	60			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=10A		10	12	mΩ
		V_{GS}=4.5V,I_D=8A		12	15	
Forward Transconductance	gfs	V_{DS}=10V,I_D=6A		11.8		S
Diode Forward Voltage	V_{SD}	I_S=1A,V_{GS} =0V			1	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=48V,V_{GS}=4.5V I_D=12A		24		nC
Gate-Source Charge	Q_{gs}			6.9		
Gate-Drain Charge	Q_{gd}			10		
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V f=1MHz		3200		pF
Output Capacitance	C_{oss}			210		
Reverse Transfer Capacitance	C_{rss}			145		
Turn-On Time	$t_{d(on)}$	V_{DD}=30V, I_D=2A,V_{GEN}=10V R_G=3.3Ω		20		nS
	t_r			4		
Turn-Off Time	$t_{d(off)}$			84.5		
	t_f			6.5		

TYPICAL CHARACTERISTICS

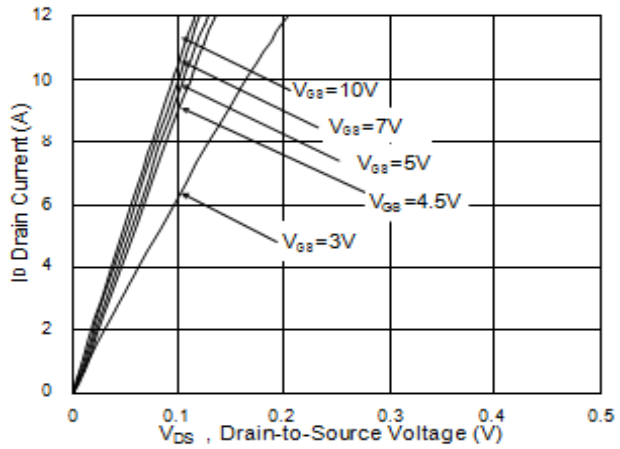

Fig. 1 Typical Output Characteristics

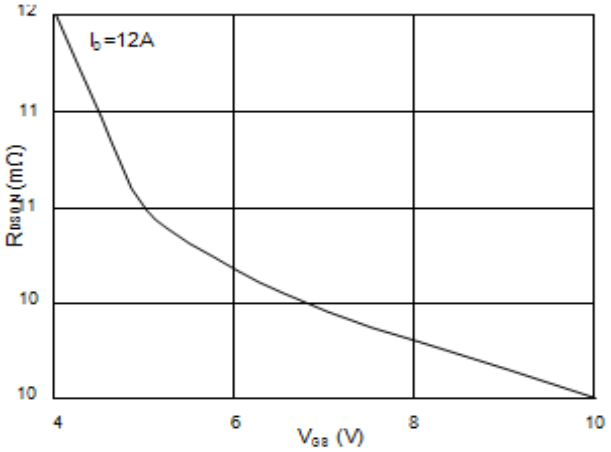

Fig. 2 On-Resistance vs. Gate Voltage

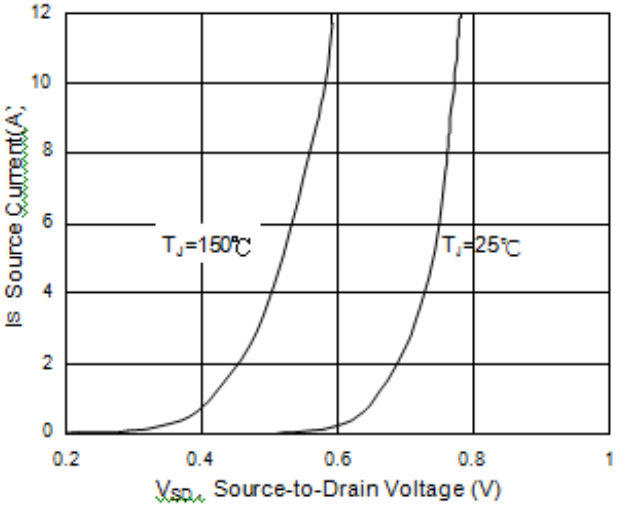

Fig. 3 Forward Characteristics Reverse Diodes

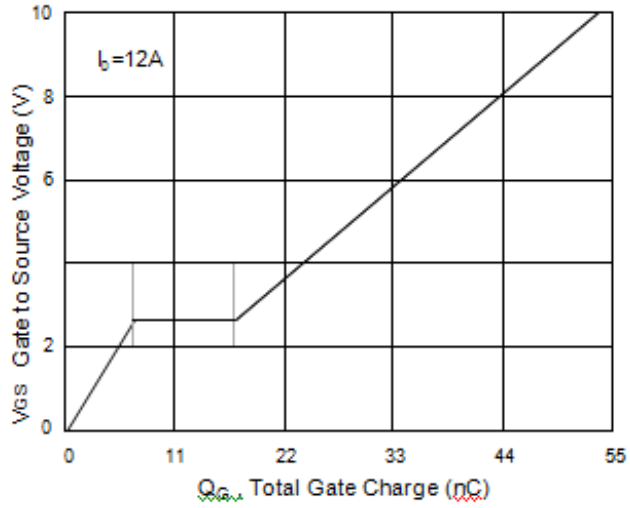

Fig. 4 Gate Charge Characteristics

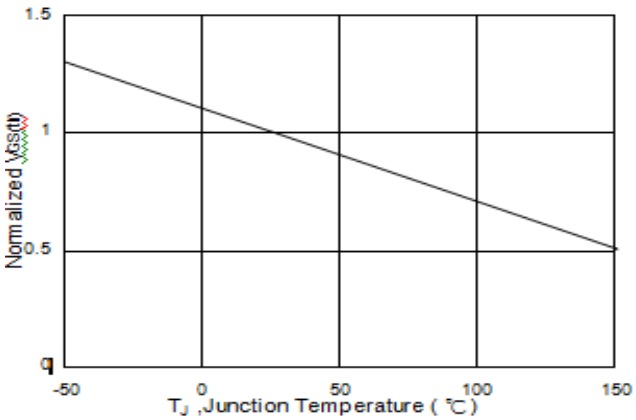

Fig. 5 Vgs vs. Junction Temperature

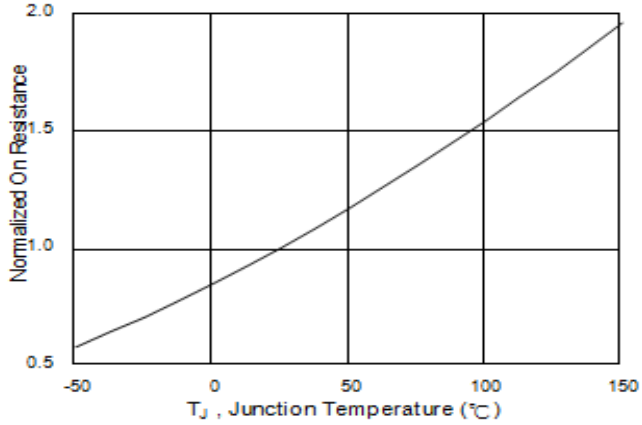

Fig. 6 On-Resistance vs. Temperature

TYPICAL CHARACTERISTICS

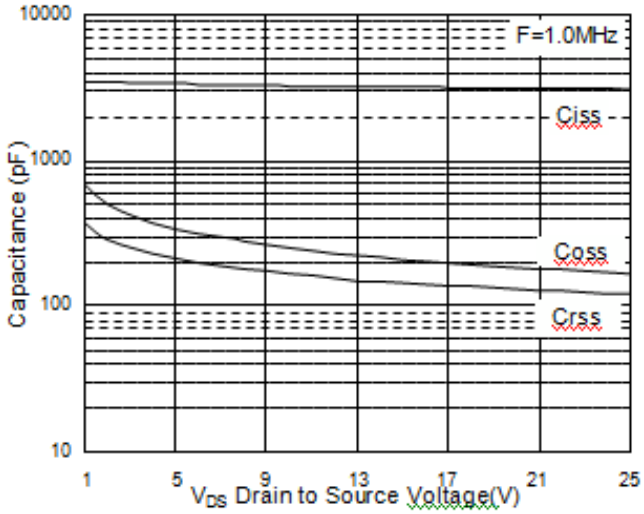

Fig. 7 Typical Capacitance Characteristics

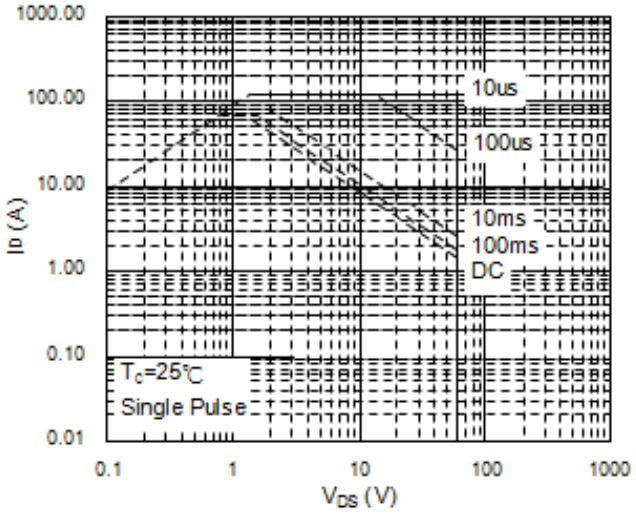

Fig. 8 Maximum Safe Operation Area

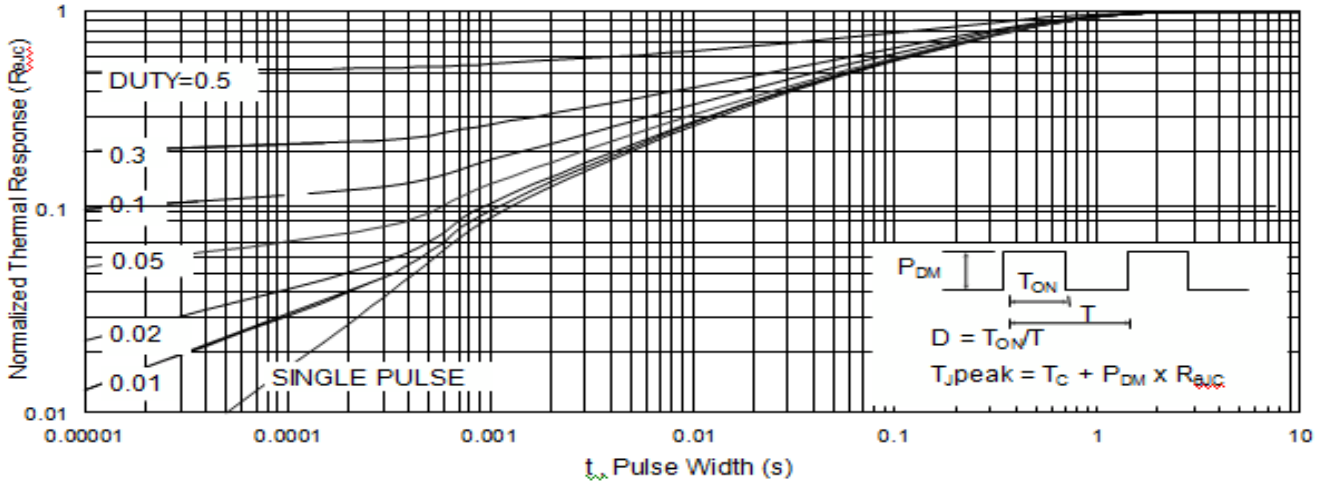

Fig. 9 Effective Transient Thermal Impedance

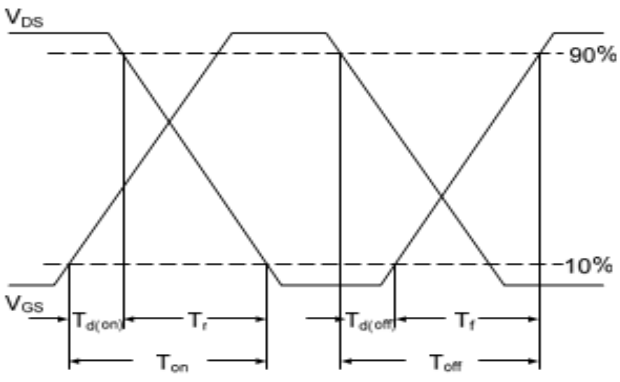

Fig. 10 Switching Time Waveform

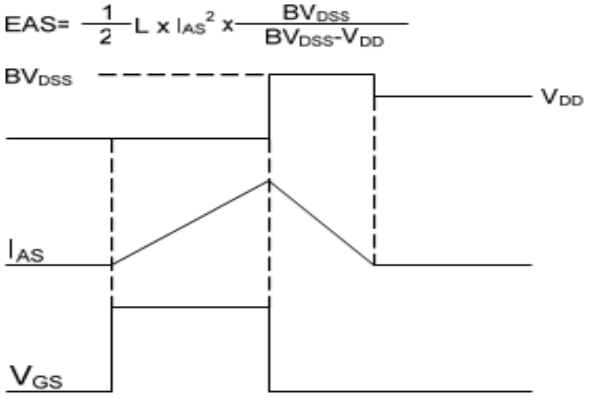

Fig. 11 Unclamped Inductive Waveform

SYNC Power Corporation
7F-2, No.3-1, Park Street
NanKang District (NKSP), Taipei, Taiwan 115
Phone: 886-2-2655-8178
Fax: 886-2-2655-8468
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