



SPN8864 N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8864 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN8864 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

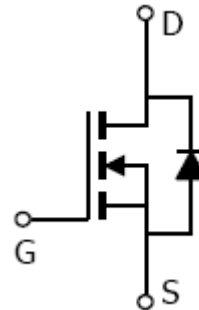
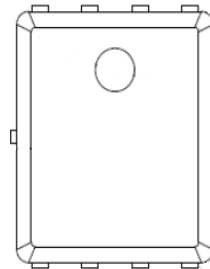
FEATURES

- ◆ 60V/20A, $R_{DS(ON)}=6.0m\Omega@V_{GS}=10V$
- ◆ 60V/20A, $R_{DS(ON)}=8.0m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK5x6-8L package design

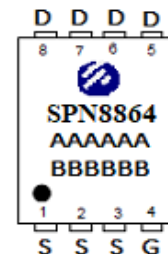
APPLICATIONS

- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

PIN CONFIGURATION(PPAK5x6-8L)



PART MARKING



A : Lot Code
B : Date Code
(YY/MM/DD)



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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8864DN8RGB	PPAK5x6-8L	SPN8864

※ SPN8864DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	60	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	I _D	T _C =25°C	85
		T _C =100°C	54
Pulsed Drain Current	I _{DM}	340	A
Single Pulse Avalanche Energy (T _C =25°C , L=0.1mH.)	E _{AS}	181	mJ
Power Dissipation	P _D	135	W
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case	R _{θJC}	0.92	°C/W



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ELECTRICAL CHARACTERISTICS

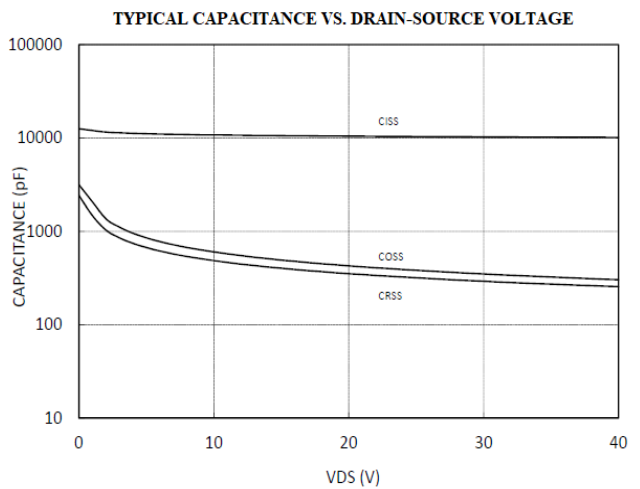
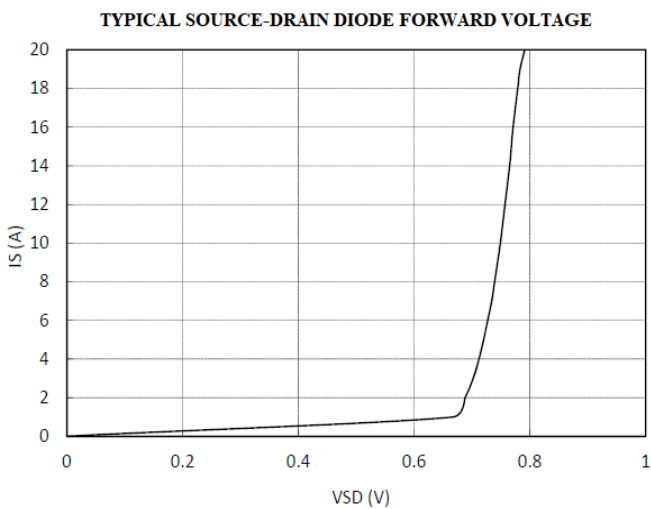
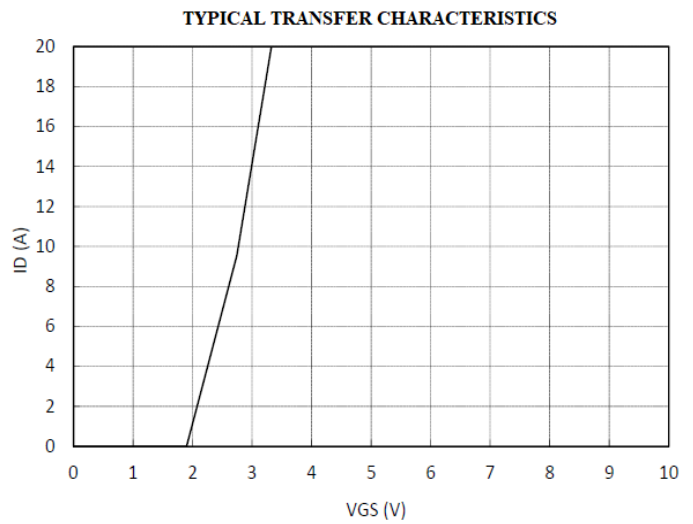
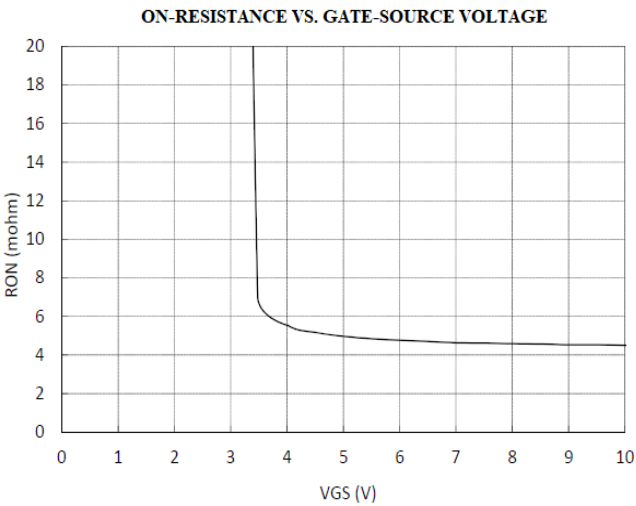
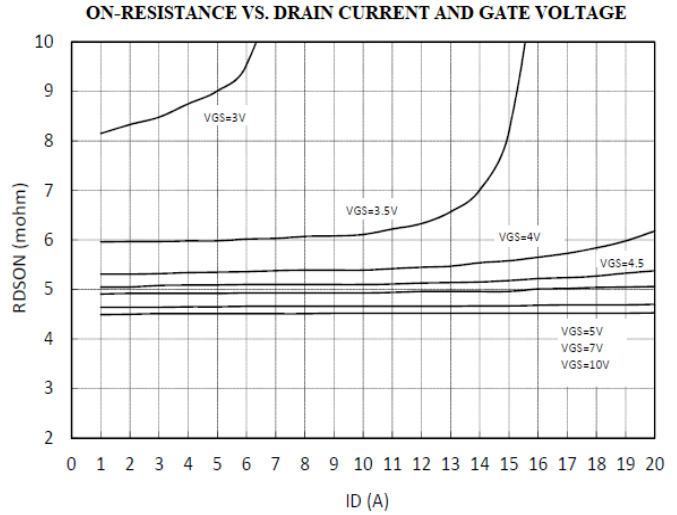
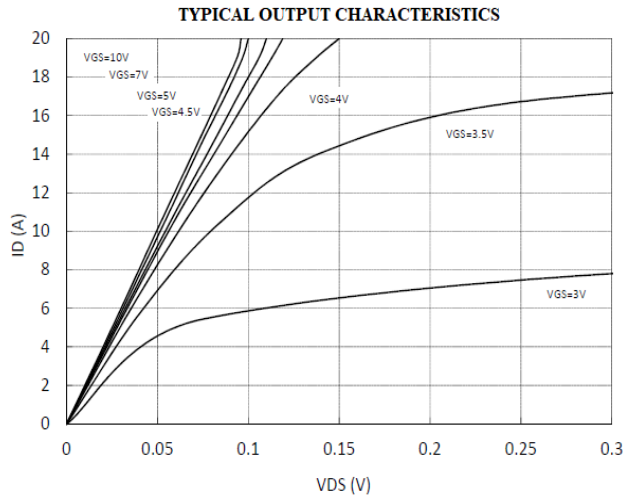
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.4	1.8	2.4	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=48V, V_{GS}=0V$			1	uA
		$V_{DS}=48V, V_{GS}=0V, T_J=125^\circ C$			10	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$			6.0	mΩ
		$V_{GS}=4.5V, I_D=20A$			8.0	
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=3A$		15		S
Gate resistance	R_g	$V_{DS}=0V, V_{GS}=0V$ $f=1MHz$		1.6		Ω
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1.0	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=30V, V_{GS}=4.5V$ $I_D=10A$		32.8	65	nC
Gate-Source Charge	Q_{gs}			10.8	20	
Gate-Drain Charge	Q_{gd}			11.6	22	
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1MHz$		10606		pF
Output Capacitance	C_{oss}			545		
Reverse Transfer Capacitance	C_{rss}			436		
Turn-On Time	$t_{d(on)}$	$V_{DD}=15V, I_D=1A, V_{GS}=10V$ $R_G=3.3\Omega$		20	40	nS
	t_r			14.2	28	
Turn-Off Time	$t_{d(off)}$			61.2	122	
	t_f			16.8	34	



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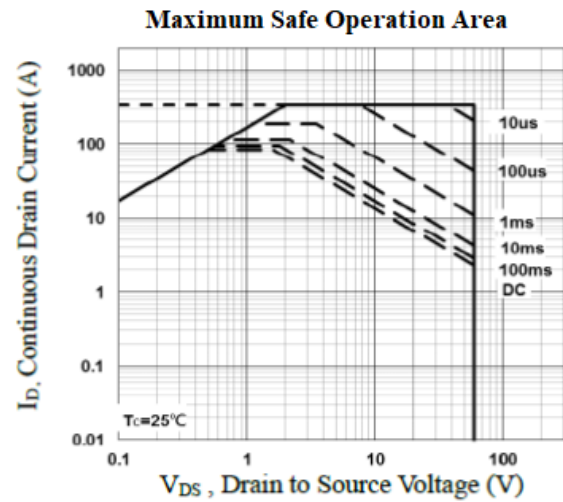
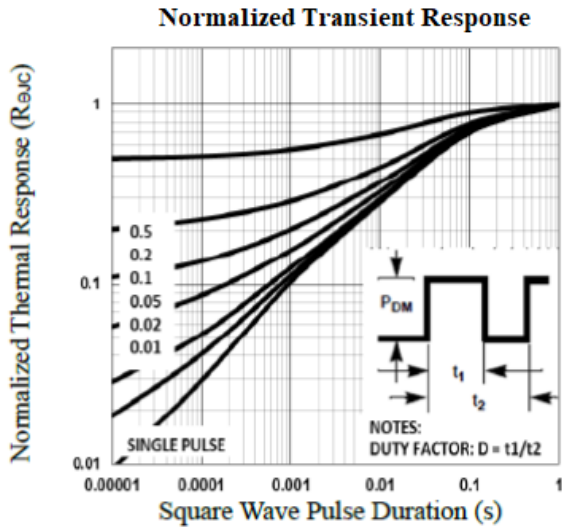
TYPICAL CHARACTERISTICS





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TYPICAL CHARACTERISTICS





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