



SPN8919

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8919 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN8910 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

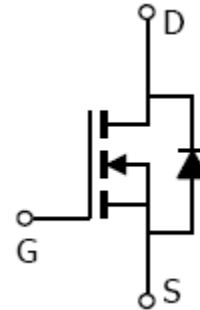
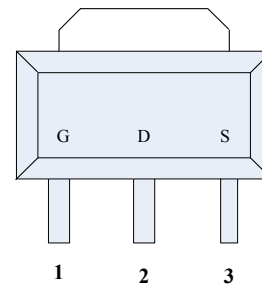
- ◆ 100V/2A, $R_{DS(ON)}= 180m\Omega@V_{GS}= 10V$
- ◆ High density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-89 package design

APPLICATIONS

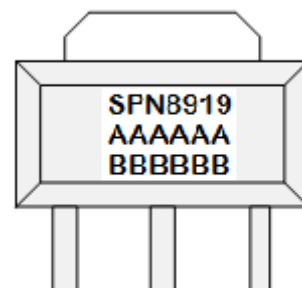
- High Frequency Small Power Switching for MB/NB/VGA
- Network DC/DC Power System
- Load Switch

PIN CONFIGURATION

SOT-89



PART MARKING





SPN8919

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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8919S89RGB	SOT-89	SPN8919

※ SPN8910S89RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	100	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	2.8	A
		TA=70°C	2.2	
Pulsed Drain Current	I _{DM}	10	A	
Power Dissipation	P _D	1.5	W	
Operating Junction Temperature	T _J	150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	85	°C/W	



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1		3.0	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V			25	μA
		V _{DS} =80V, V _{GS} =0V T _J =125°C			250	
On-State Drain Current	I _{D(on)}	V _{DS} ≥5V, V _{GS} =10V	2.2			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =2A		0.160	0.180	Ω
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =5A		5.6		S
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V			1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =50V, V _{GS} =10V I _D =2A		10	16	nC
Gate-Source Charge	Q _{gs}			2.5		
Gate-Drain Charge	Q _{gd}			4.5		
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V f=1MHz		430		pF
Output Capacitance	C _{oss}			56		
Reverse Transfer Capacitance	C _{rss}			35		
Turn-On Time	t _{d(on)}	V _{DD} =50V, I _D =2A, V _{GEN} =10V, R _G =3.3Ω		6.5		nS
	t _r			10		
Turn-Off Time	t _{d(off)}			13		
	t _f			3.4		



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TYPICAL CHARACTERISTICS

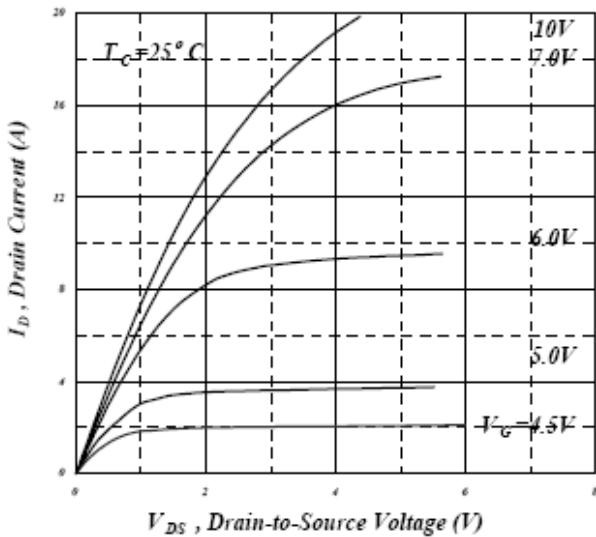


Fig 1. Typical Output Characteristics

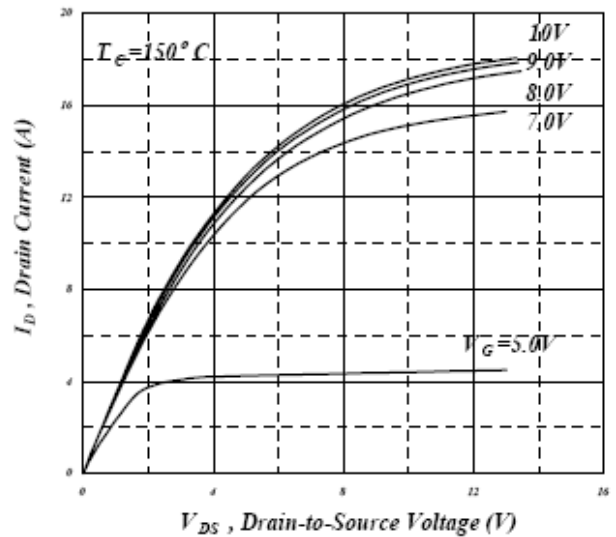


Fig 2. Typical Output Characteristics

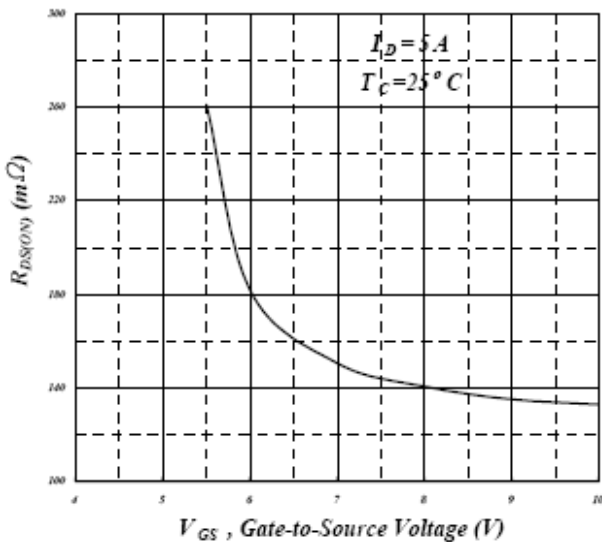


Fig 3. On-Resistance v.s. Gate Voltage

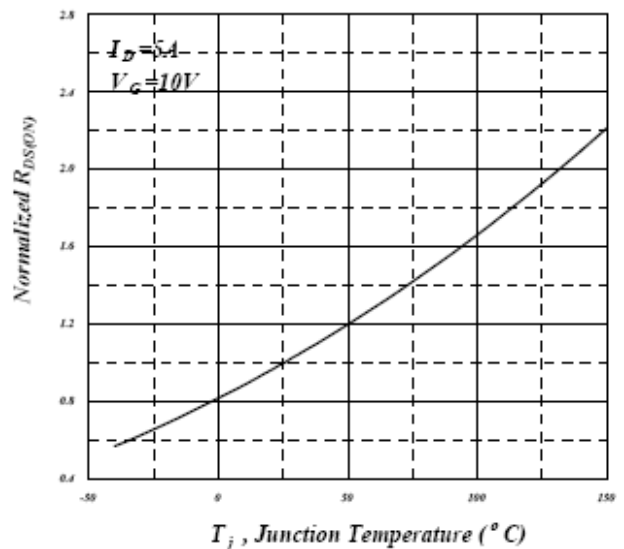


Fig 4. Normalized On-Resistance v.s. Junction Temperature



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TYPICAL CHARACTERISTICS

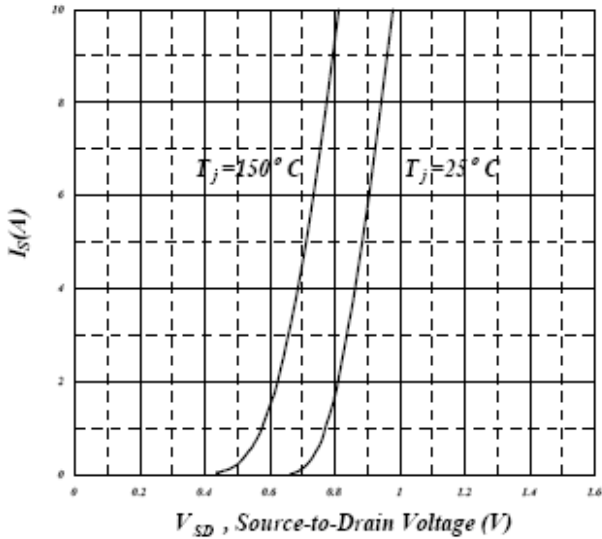


Fig 5. Forward Characteristic of Reverse Diode

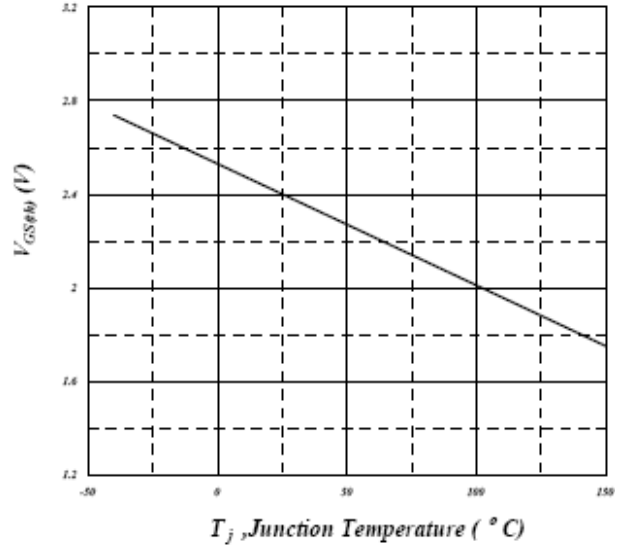


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

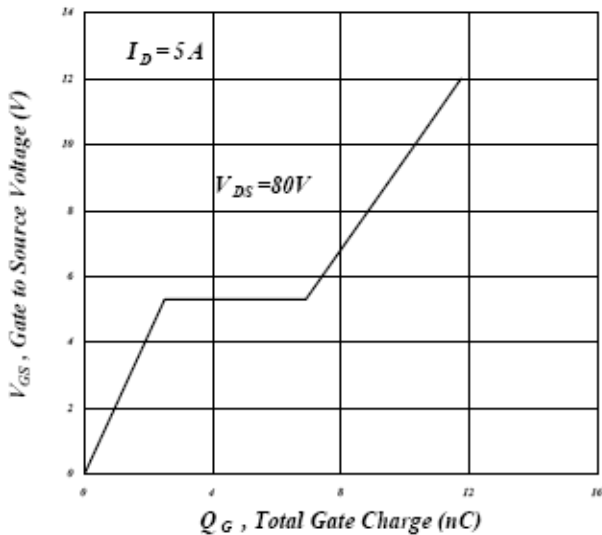


Fig 7. Gate Charge Characteristics

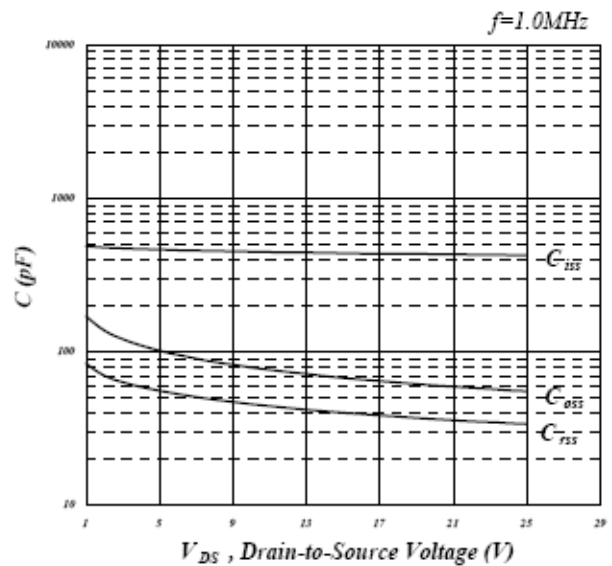


Fig 8. Typical Capacitance Characteristics



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TYPICAL CHARACTERISTICS

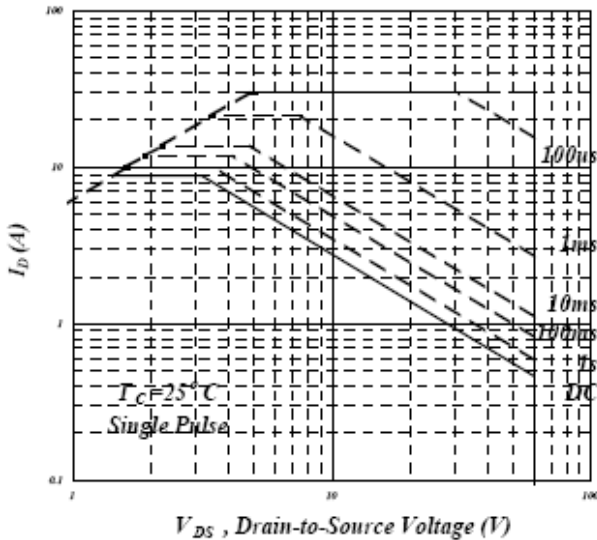


Fig 9. Maximum Safe Operating Area

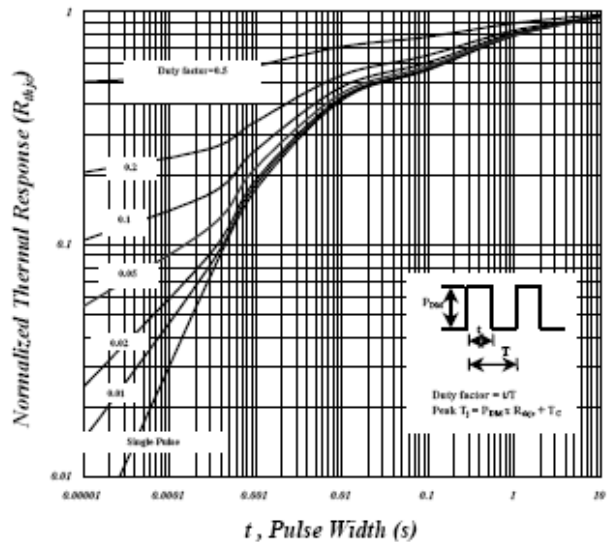


Fig 10. Effective Transient Thermal Impedance

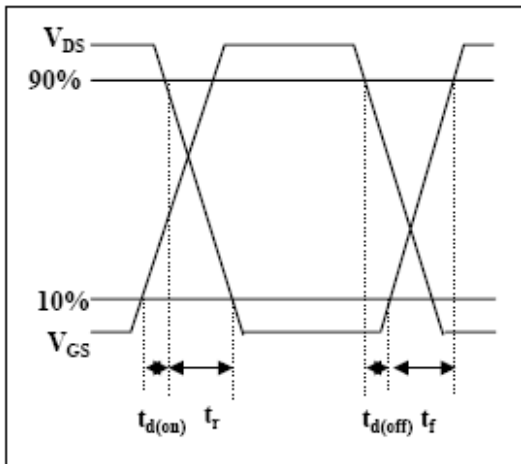


Fig 11. Switching Time Waveform

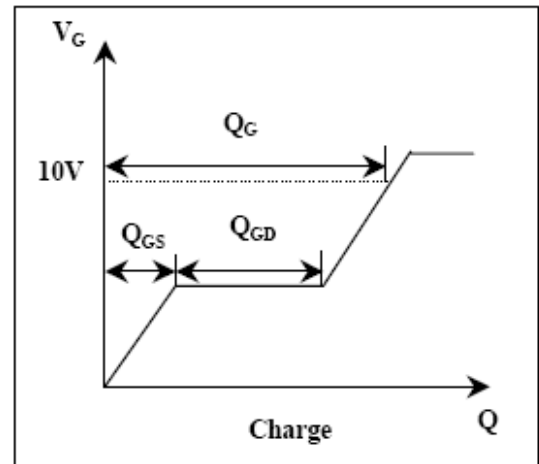


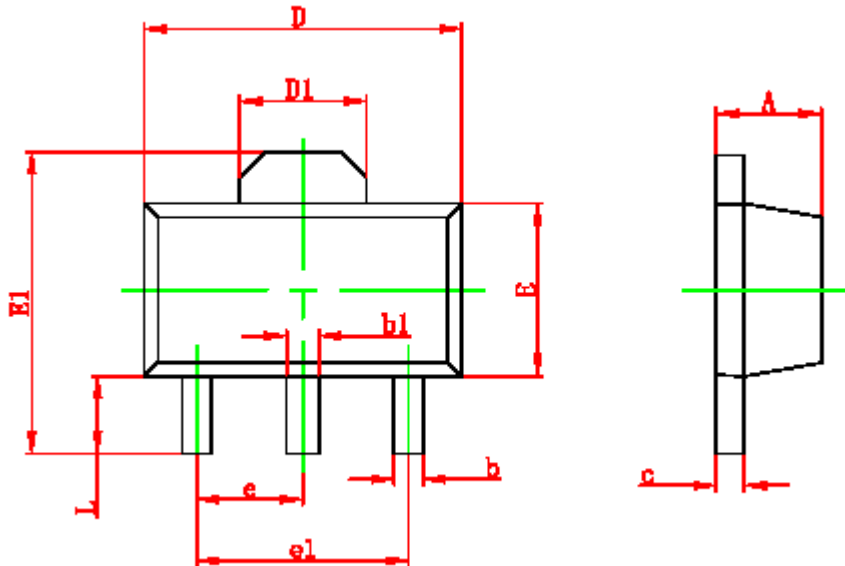
Fig 12. Gate Charge Waveform



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SOT-89 PACKAGE OUTLINE



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047



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