SPN90N08
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN90N08 is the N-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching is required.

APPLICATIONS

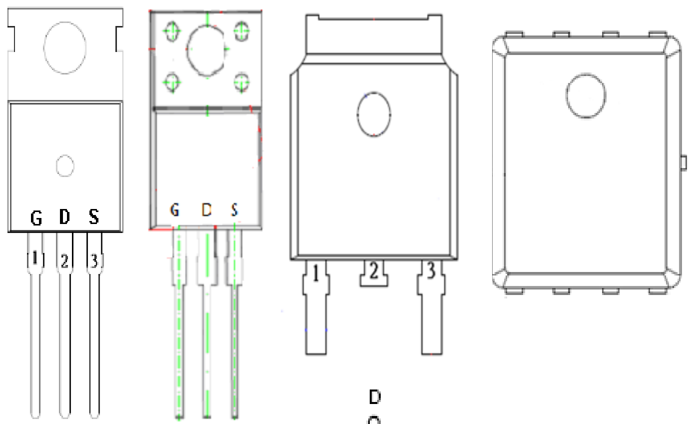
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

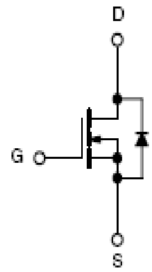
FEATURES

- ◆ 80V/95A,$R_{DS(ON)}$=5.9mΩ@V_{GS}=10V
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L/TO-220F-3L/TO-252-2L/ PPAK5x6-8L package design

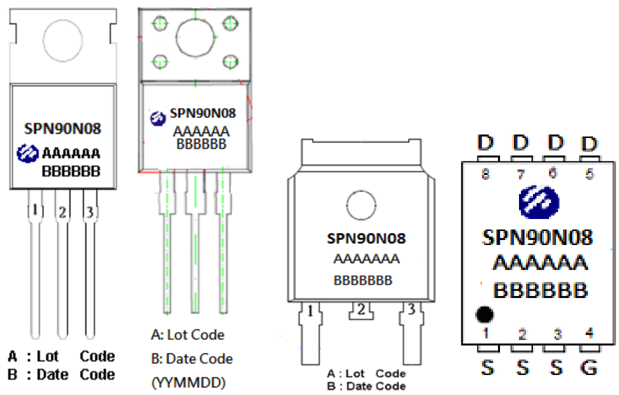
PIN CONFIGURATION (PPAK5x6-8L)

TO-220 TO-220F TO-252 PPAK5x6





PART MARKING



PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PIN DESCRIPTION (PPAK5x6-8L)

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN90N08T220TGB	TO-220-3L	SPN90N08
SPN90N08T220FTGB	TO-220F-3L	SPN90N08
SPN90N08T252RGB	TO-252-2L	SPN90N08
SPN90N08DN8RGB	PPAK5x6-8L	SPN90N08

※ SPN90N08T220TGB : Tube ; Pb – Free ; Halogen – Free
※ SPN90N08T220FTGB : Tube ; Pb – Free ; Halogen – Free
※ SPN90N08T252RGB : Tape&Reel ; Pb – Free ; Halogen - Free
※ SPN90N08DN8RGB : 13” Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	80	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	T_C=25℃	I_D	95	A
	T_C=100℃		70	
Pulsed Drain Current		I_{DM}	280	A
Avalanche Energy with Single Pulse (T_C=25℃, L=0.1mH.)		E_{AS}	174	mJ
Power Dissipation@ Tc=25℃	TO-220	P_D	104	W
Power Dissipation@ Tc=25℃	TO-252/TO-220F		93	
Power Dissipation@ Tc=25℃	PPAK5x6		83	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case (TO-220/TO-220F)		$R_{\theta JC}$	1.2	℃/W
Thermal Resistance-Junction to Case (TO-251S/TO-252)		$R_{\theta JC}$	1.35	℃/W
Thermal Resistance-Junction to Case (PPAK5x6)		$R_{\theta JC}$	1.5	℃/W

Note :

The maximum current rating is package limited at 120A for TO-220-3L
The maximum current rating is package limited at 78A for TO-220F-3L
The maximum current rating is package limited at 70A for TO-252-2L
The maximum current rating is package limited at 80A for PPAK5x6-8L

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	80			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2.0	2.7	4.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=64V,V_{GS}=0V, T_J=25℃			1	uA
		V_{DS}=64V,V_{GS}=0V, T_J=100℃			100	uA
Gate Resistance	R_G	V_{GS}=0V,V_{DS} open, f=1MHz		1.1		Ω
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=15A		5.2	5.9	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		50		S
Dynamic						
Total Gate Charge	Q_g	V_{DS}=40V,V_{GS}=10V I_D=20A		41		nC
Gate-Source Charge	Q_{gs}			10		nC
Gate-Drain Charge	Q_{gd}			10		nC
Input Capacitance	C_{iss}	V_{DS}=40V,V_{GS}=0V f=1MHz		2373		pF
Output Capacitance	C_{oss}			769		pF
Reverse Transfer Capacitance	C_{rss}			45		pF
Turn-On Time	$t_{d(on)}$	V_{DD}=40V, I_D=20A,V_{GS}=10V R_G=10Ω		11		nS
	t_r			7		nS
Turn-Off Time	$t_{d(off)}$			35		nS
	t_f			9		nS
Reverse Diodes						
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		1.0	1.2	V
Reverse Recovery Time	t_{rr}	V_R = 80V, I_S=20A, dIs/dt =400A/uS		35		nS
Reverse Recovery Charge	Q_{rr}			120		nC

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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

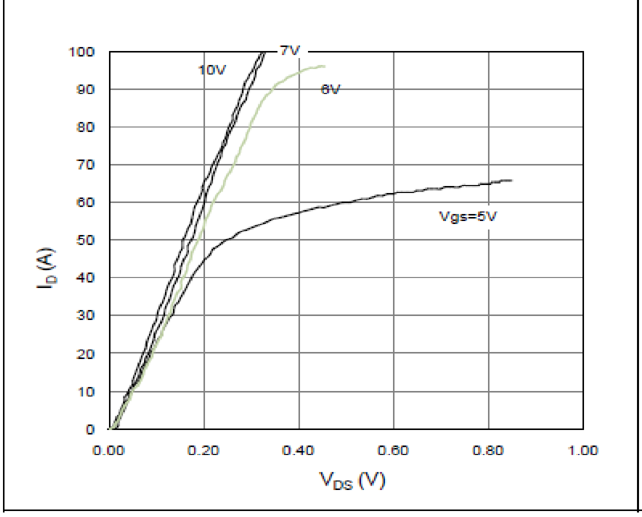


Figure 2. On-Resistance vs. Gate-Source Voltage

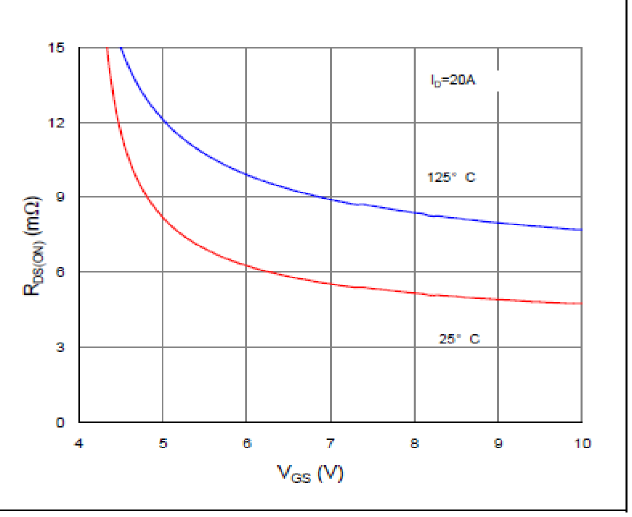


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

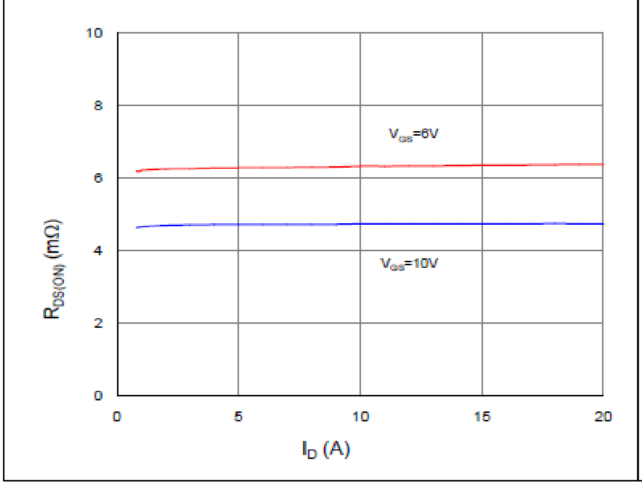


Figure 4. Normalized On-Resistance vs. Junction Temperature

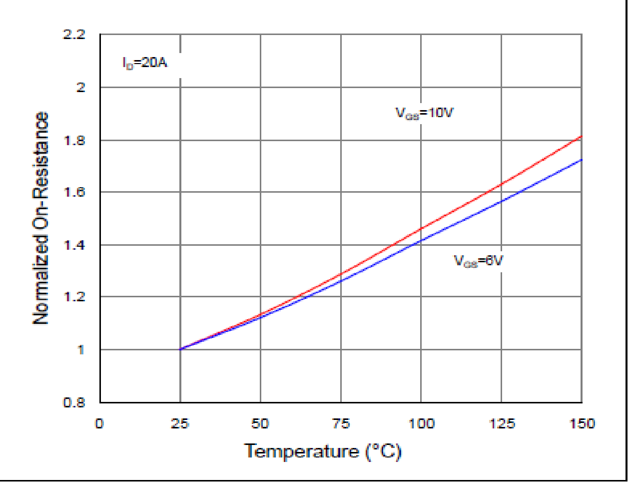


Figure 5. Typical Transfer Characteristics

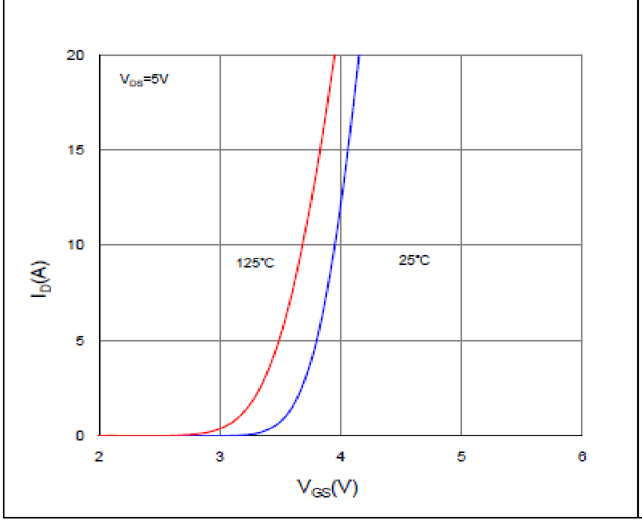
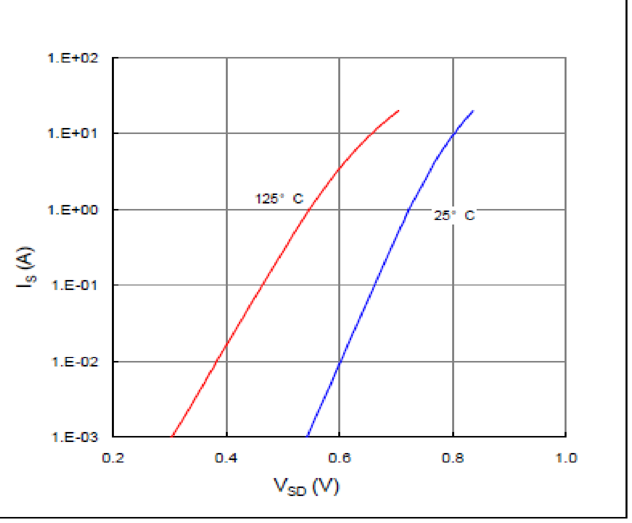


Figure 6. Typical Source-Drain Diode Forward Voltage



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TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

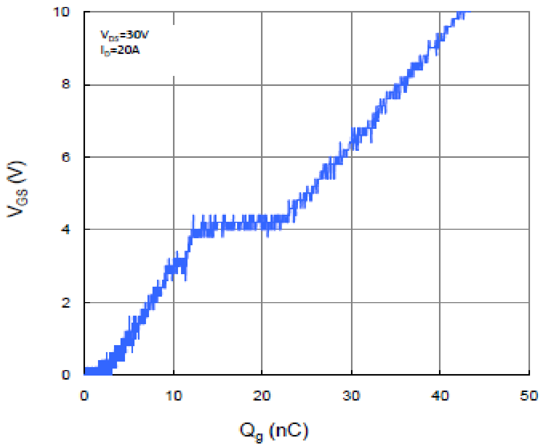


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

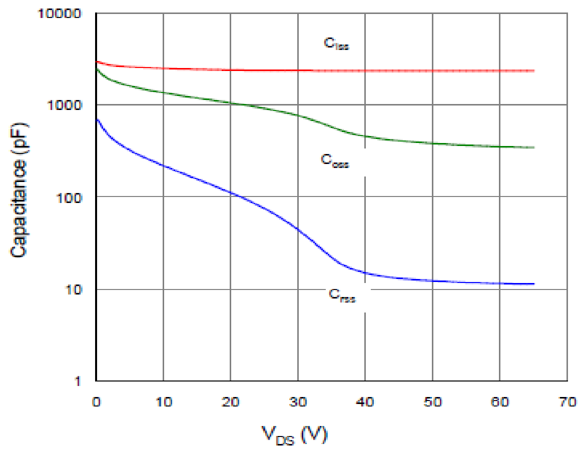


Figure 9. Maximum Safe Operating Area

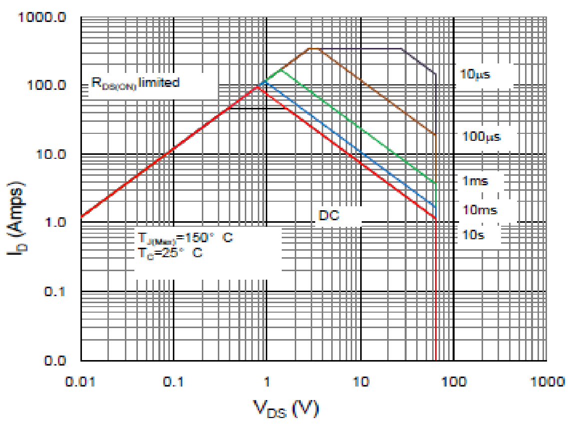


Figure 10. Maximun Drain Current vs. Case Temperature

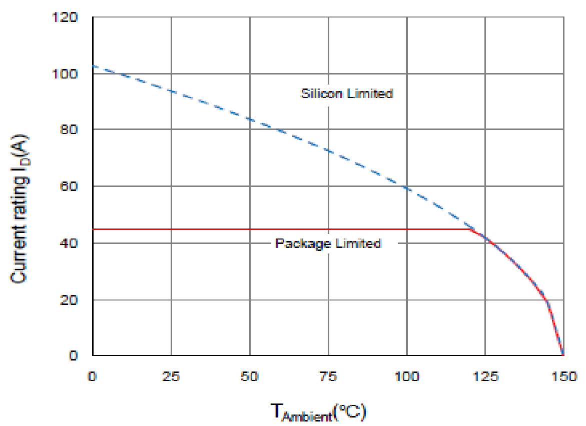
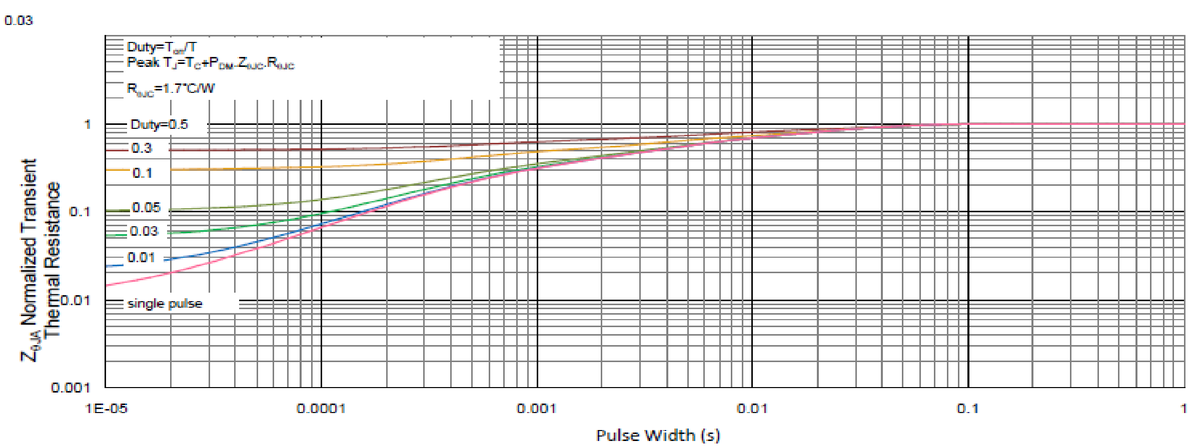


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



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