



SPN9507

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN9507 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

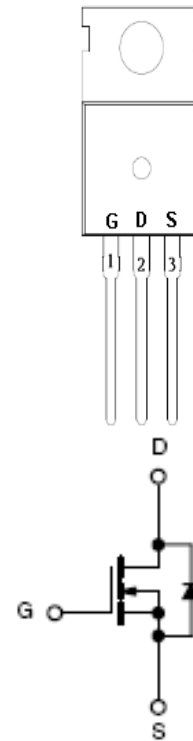
FEATURES

- ◆ 75V/60A, $R_{DS(ON)}=5.0m\Omega@V_{GS}=10V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L package design

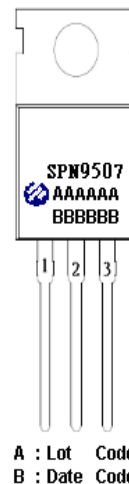
APPLICATIONS

- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier

PIN CONFIGURATION(TO-220-3L)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN9507T220TGB	TO-220-3L	SPN9507

※ SPN9507T220TGB: Tube ; Pb – Free; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	75	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	80	A
		TA=70°C	70	
Pulsed Drain Current	I _{DM}	240	A	
Power Dissipation	P _D	TA=25°C	300	W
		TA=70°C	3.38	
Avalanche Energy with Single Pulse (T _j =25°C , L = 0.12mH , I _{AS} = 80A , V _{DD} = 60V.)	EAS	380	mJ	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	2	°C/W	



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ELECTRICAL CHARACTERISTICS

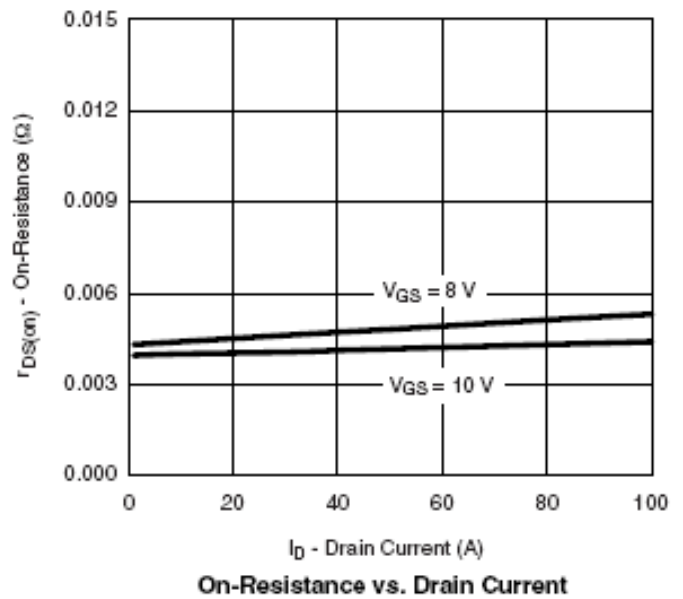
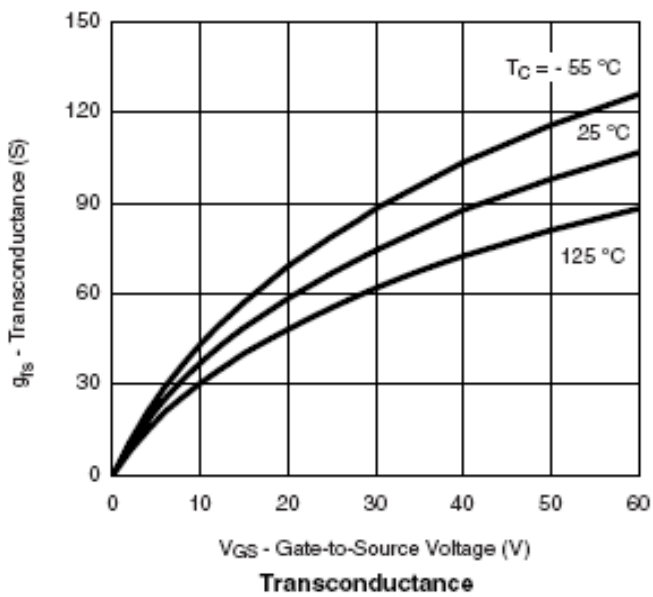
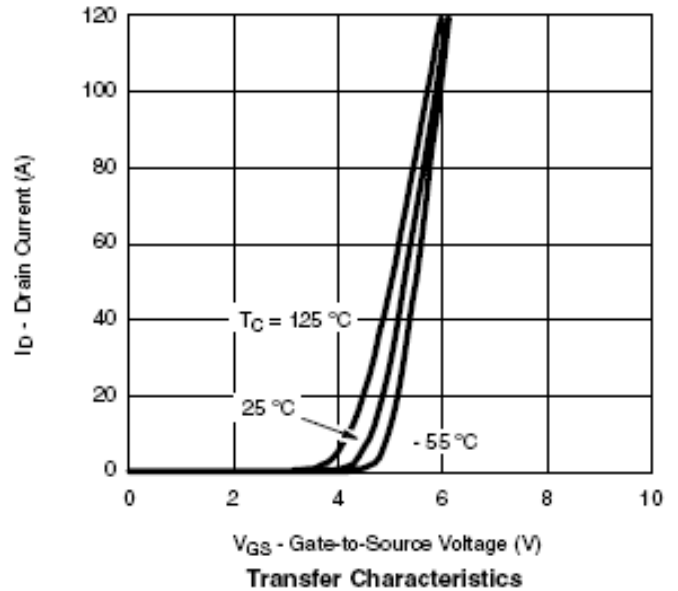
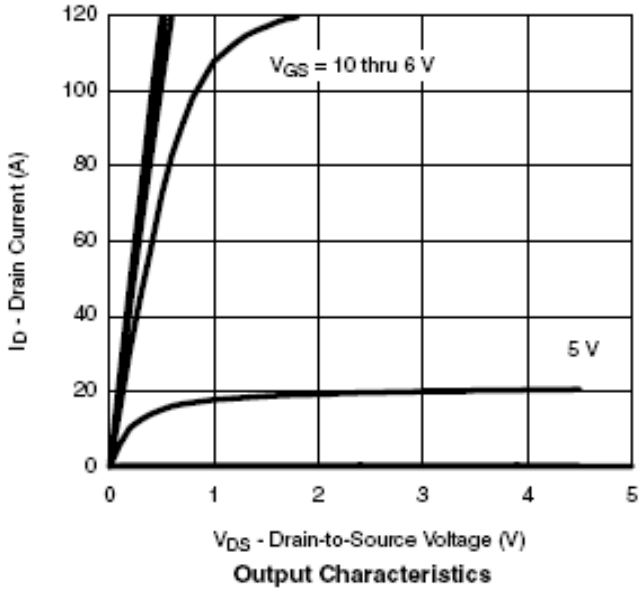
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	75			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=75V, V_{GS}=0V$			10	uA
		$V_{DS}=60V, V_{GS}=0V$ $T_J = 150^\circ C$			250	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=60A$			5.0	mΩ
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=60A$		57		S
Diode Forward Voltage	V_{SD}	$I_S=60A, V_{GS}=0V$			1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=40V, V_{GS}=10V$ $I_D=80A$		85	135	nC
Gate-Source Charge	Q_{gs}			25		
Gate-Drain Charge	Q_{gd}			36		
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1MHz$		4290	6870	pF
Output Capacitance	C_{oss}			985		
Reverse Transfer Capacitance	C_{rss}			390		
Turn-On Time	$t_{d(on)}$	$V_{DD}=40V, R_L=0.5\Omega$ $I_D=80A, V_{GEN}=10V$ $R_G=3.3\Omega$		22		nS
	t_r			160		
Turn-Off Time	$t_{d(off)}$			38		
	t_f			165		



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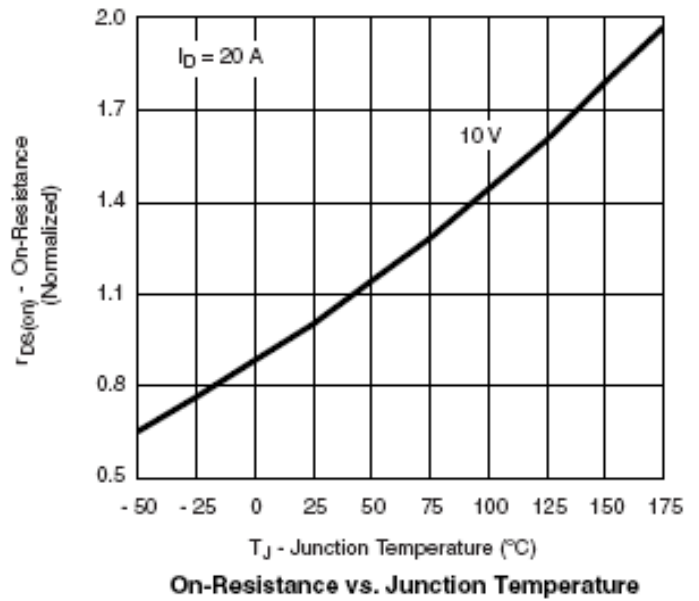
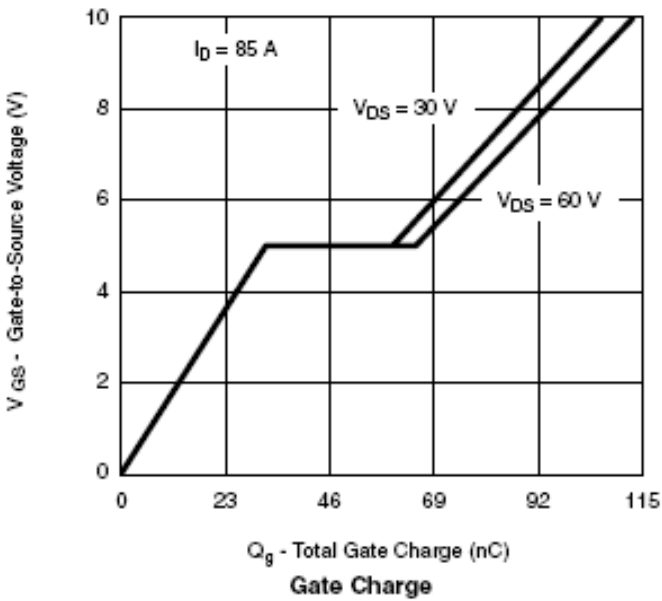
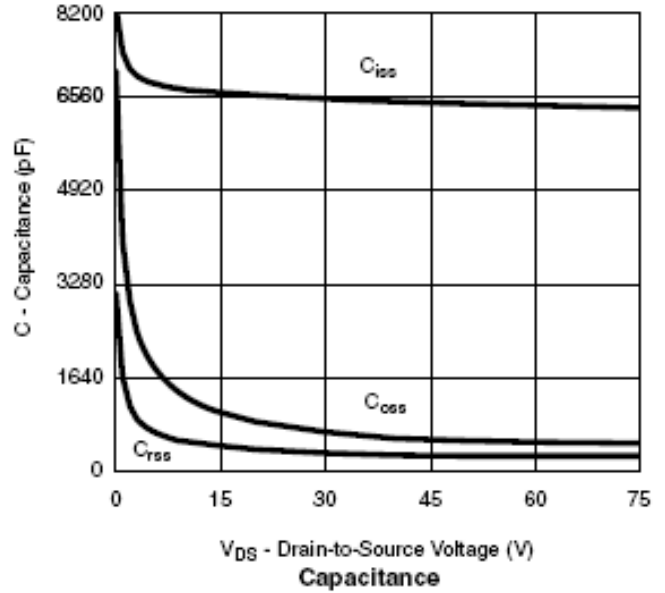
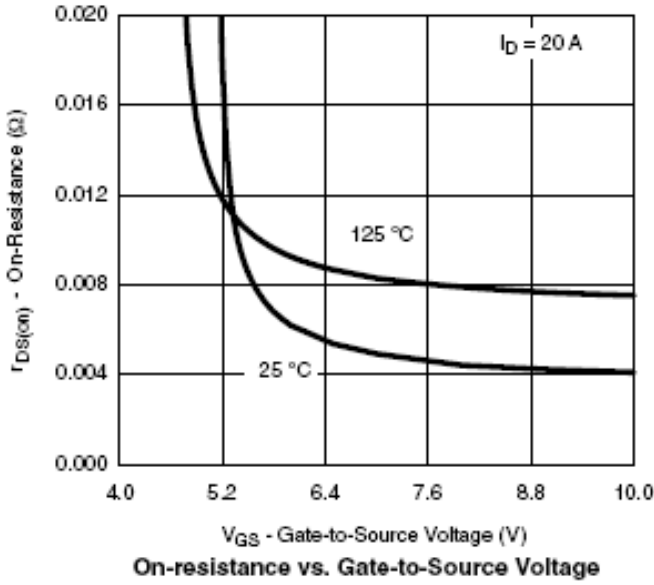
TYPICAL CHARACTERISTICS





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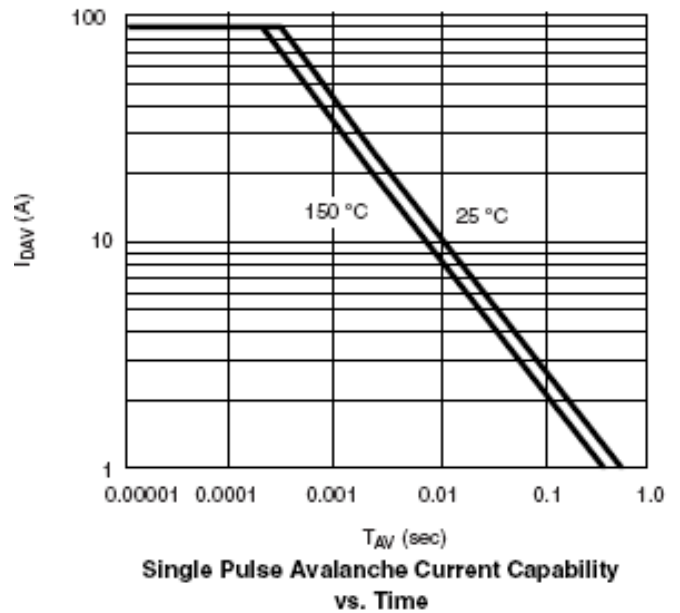
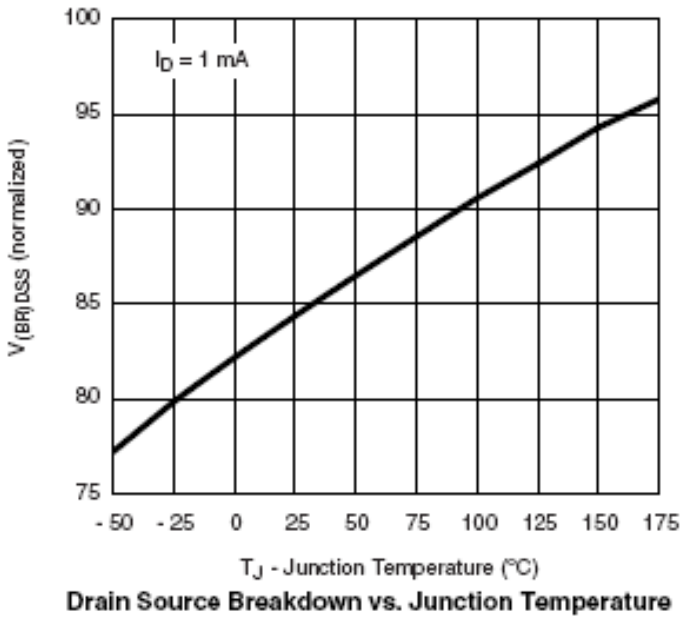
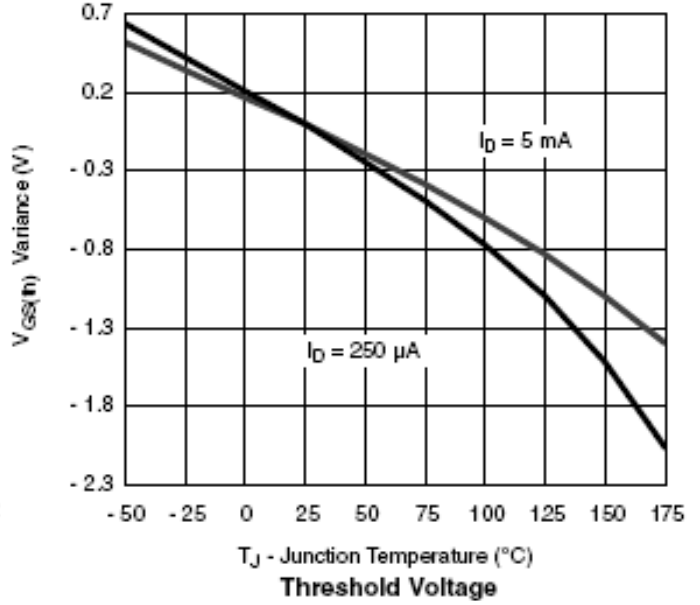
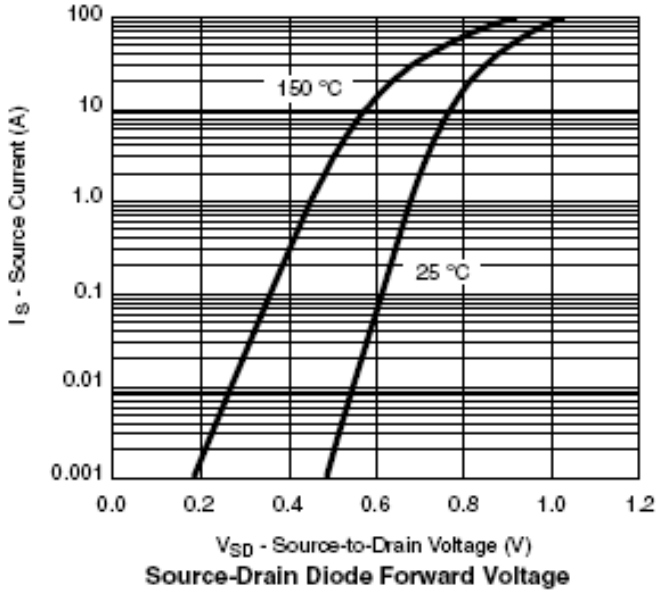




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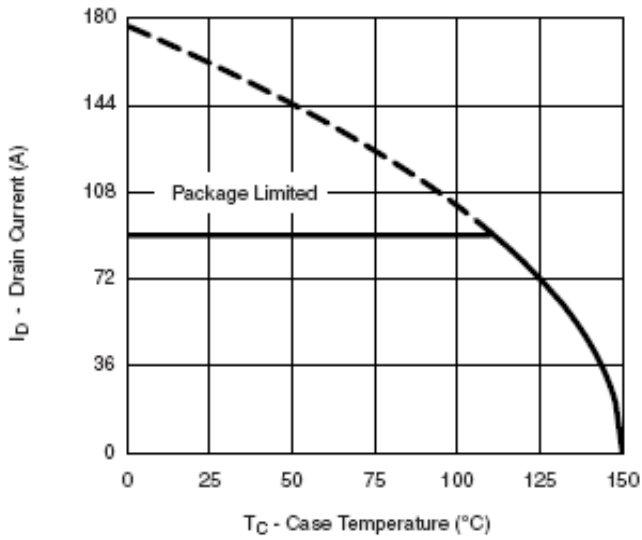
TYPICAL CHARACTERISTICS



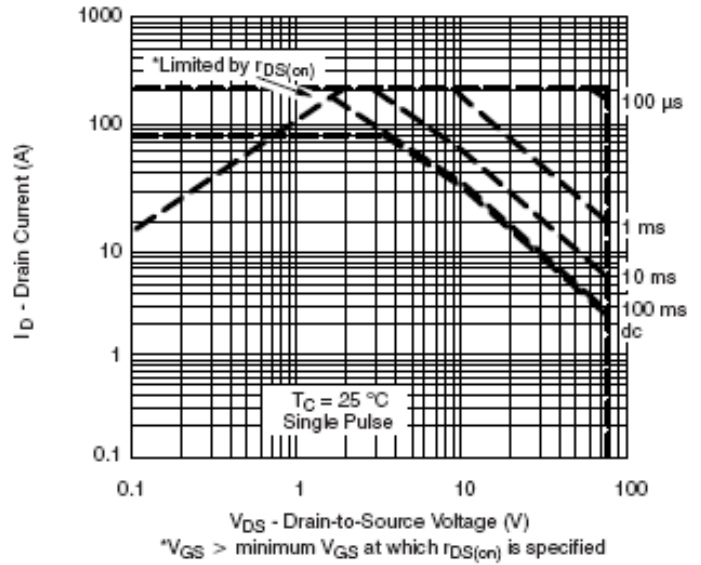


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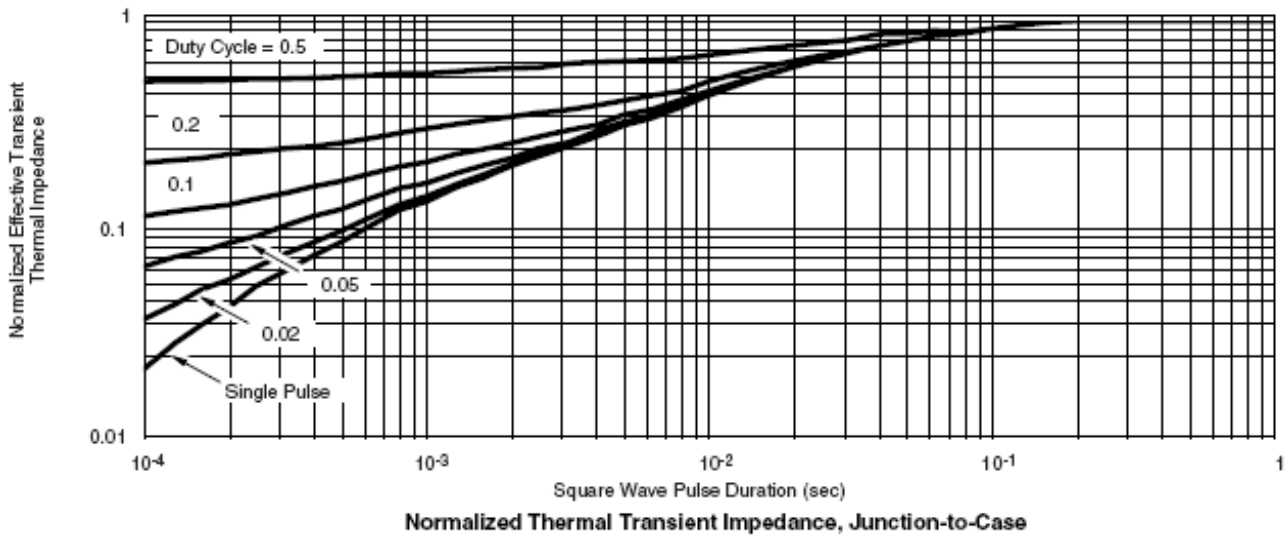
TYPICAL CHARACTERISTICS



Maximum Drain Current vs. Case Temperature



Safe Operating Area



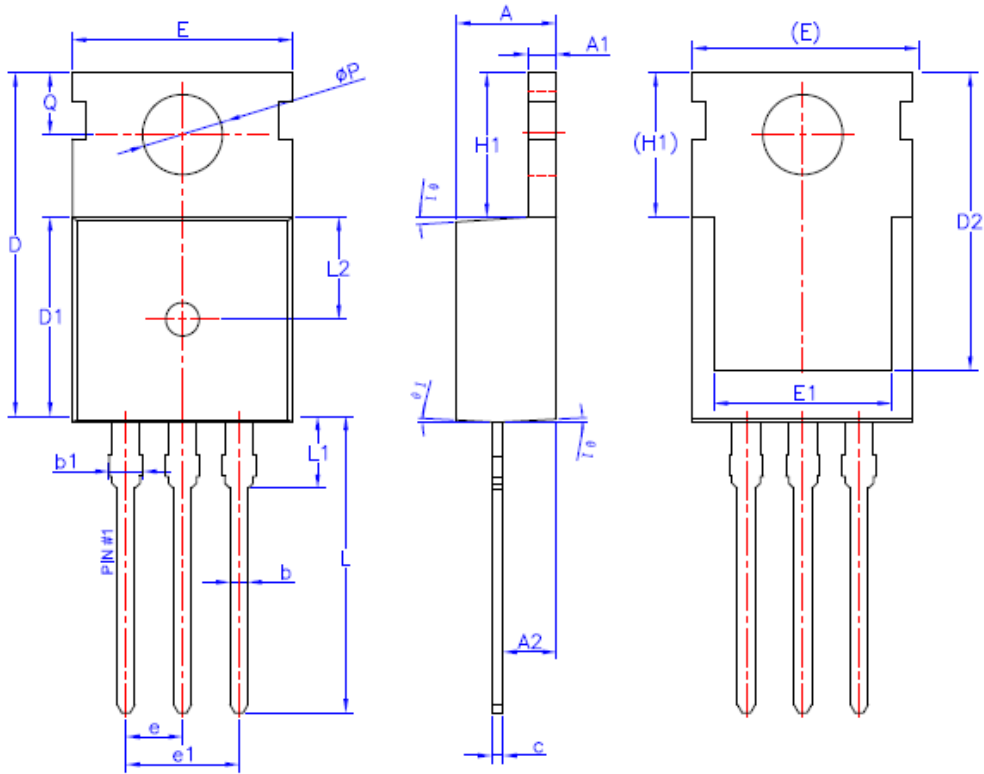
Normalized Thermal Transient Impedance, Junction-to-Case



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TO-220-3L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	—	0.90
b1	1.42	—	1.57
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	—	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	—	—	3.50
L2	4.60REF		
φP	3.55	3.60	3.65
Q	2.73	—	2.87
φ1	1°	3°	5°



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