



# SPN9928

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN9928 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

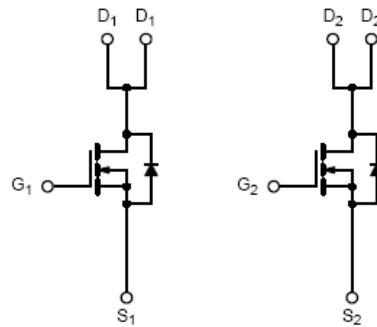
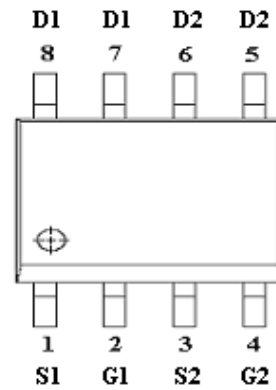
### FEATURES

- ◆ 20V/6.0A,  $R_{DS(ON)}=25m\Omega@V_{GS}=4.5V$
- ◆ 20V/5.0A,  $R_{DS(ON)}=32m\Omega@V_{GS}=2.5V$
- ◆ 20V/4.0A,  $R_{DS(ON)}=50m\Omega@V_{GS}=1.8V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

### PIN CONFIGURATION(SOP – 8P)



### PART MARKING



A : Lot Code  
B : Date Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN9928S8RGB	SOP- 8P	SPN9928

※ SPN9928S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	20	V	
Gate –Source Voltage	V <sub>GSS</sub>	±12	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	6.8	A
		TA=70°C	4.8	
Pulsed Drain Current	I <sub>DM</sub>	30	A	
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	1.6	A	
Power Dissipation	P <sub>D</sub>	TA=25°C	2.8	W
		TA=70°C	1.8	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	105	°C/W	



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### ELECTRICAL CHARACTERISTICS

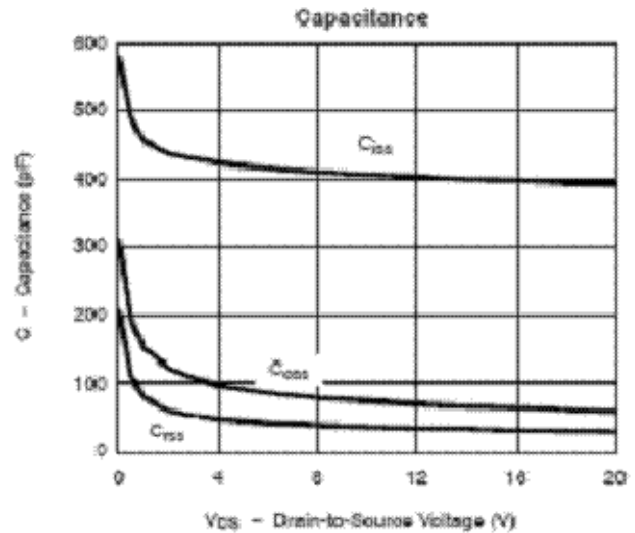
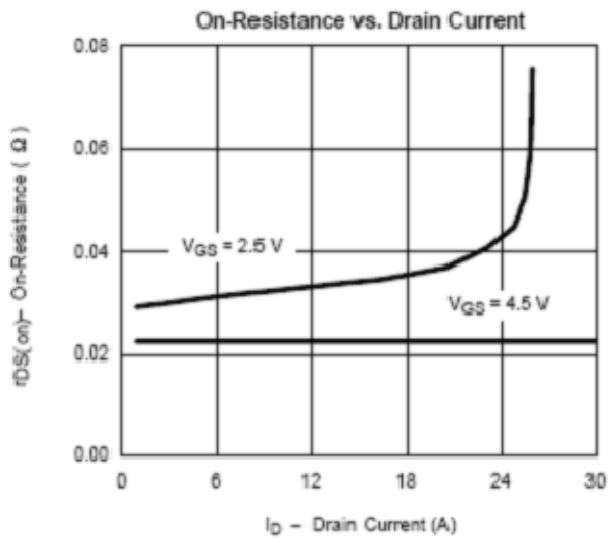
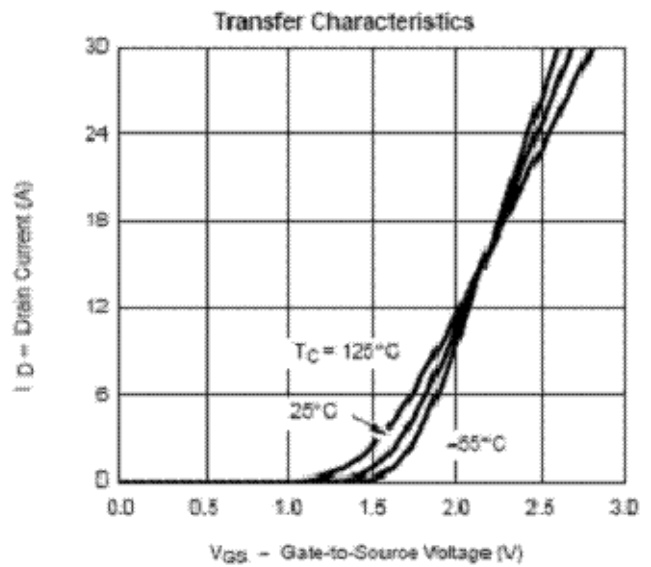
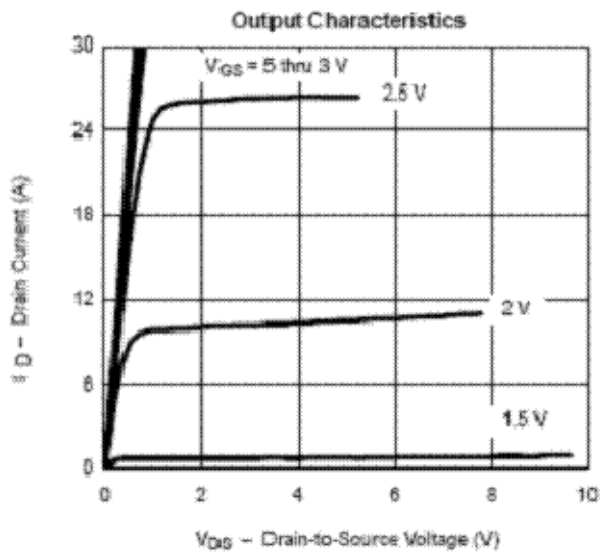
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5		1.0	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=20V, V_{GS}=0V$			1	uA
		$V_{DS}=20V, V_{GS}=0V$ $T_J=55^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq 5V, V_{GS}=4.5V$	6			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=6.0A$		0.023	0.025	$\Omega$
		$V_{GS}=2.5V, I_D=5.0A$		0.028	0.032	
		$V_{GS}=1.8V, I_D=4.0A$		0.040	0.050	
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=-3.6A$		10		S
Diode Forward Voltage	$V_{SD}$	$I_S=1.7A, V_{GS}=0V$		0.8	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=10V, V_{GS}=4.5V,$ $I_D=6.0A$		2		nC
Gate-Source Charge	$Q_{gs}$			2.5		
Gate-Drain Charge	$Q_{gd}$			2.1		
Input Capacitance	$C_{iss}$	$V_{DS}=8V, V_{GS}=0V$ $f=1MHz$		575		pF
Output Capacitance	$C_{oss}$			84		
Reverse Transfer Capacitance	$C_{rss}$			22		
Turn-On Time	$t_{d(on)}$	$V_{DD}=10V, R_L=6\Omega$ $I_D=1.0A, V_{GEN}=4.5V$ $R_G=6\Omega$		10	14	ns
	$t_r$			16	20	
Turn-Off Time	$t_{d(off)}$			35	40	
	$t_f$			3	10	



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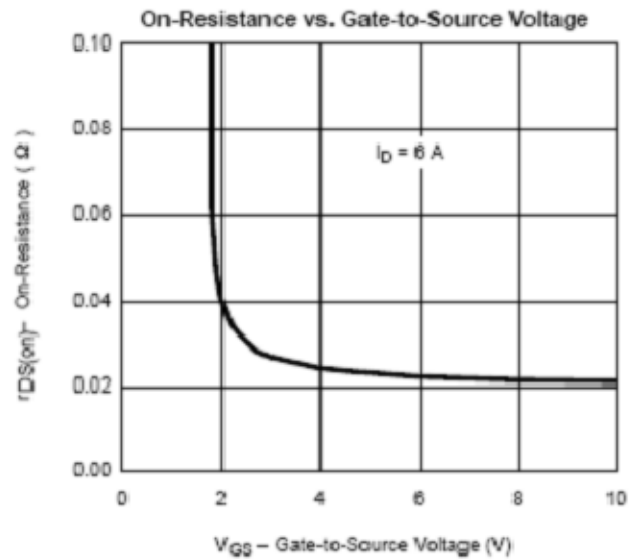
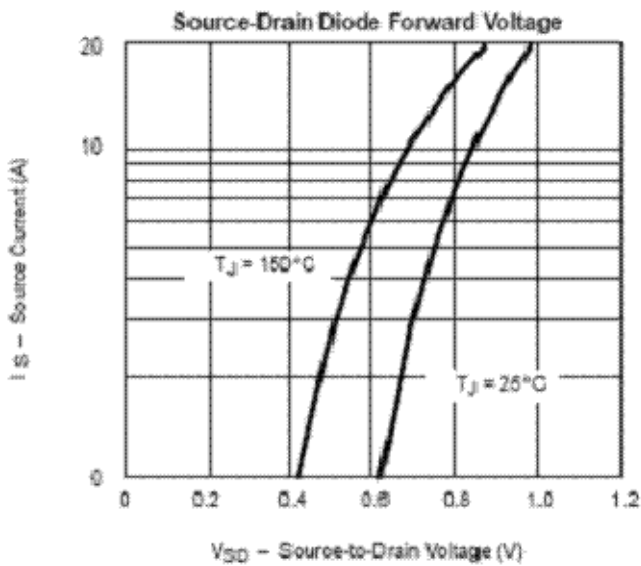
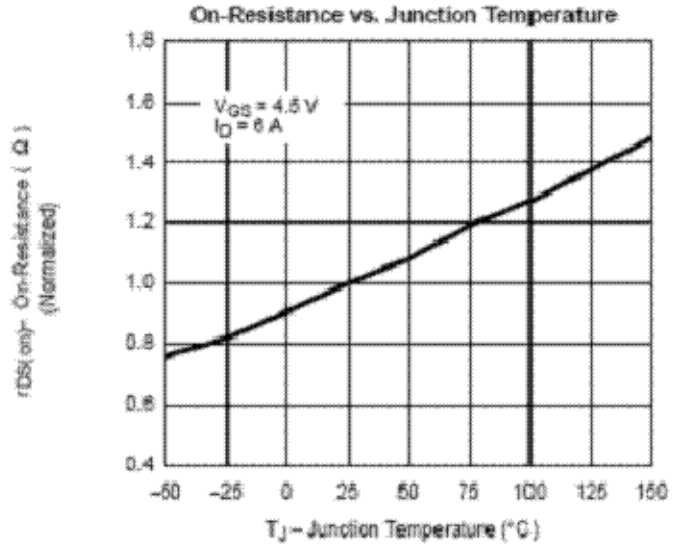
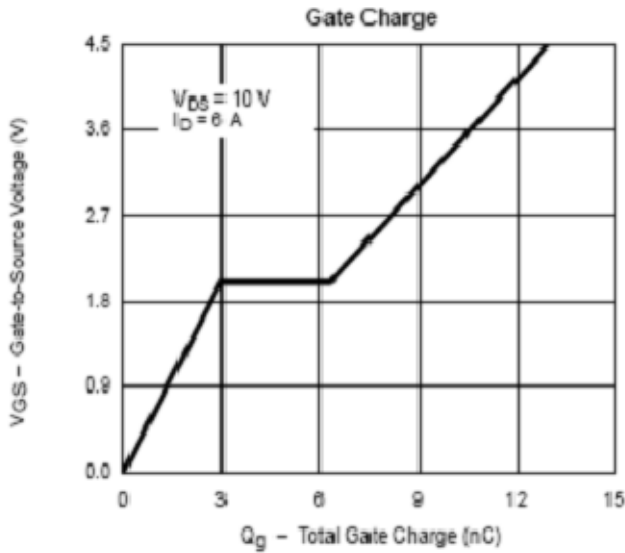
## TYPICAL CHARACTERISTICS





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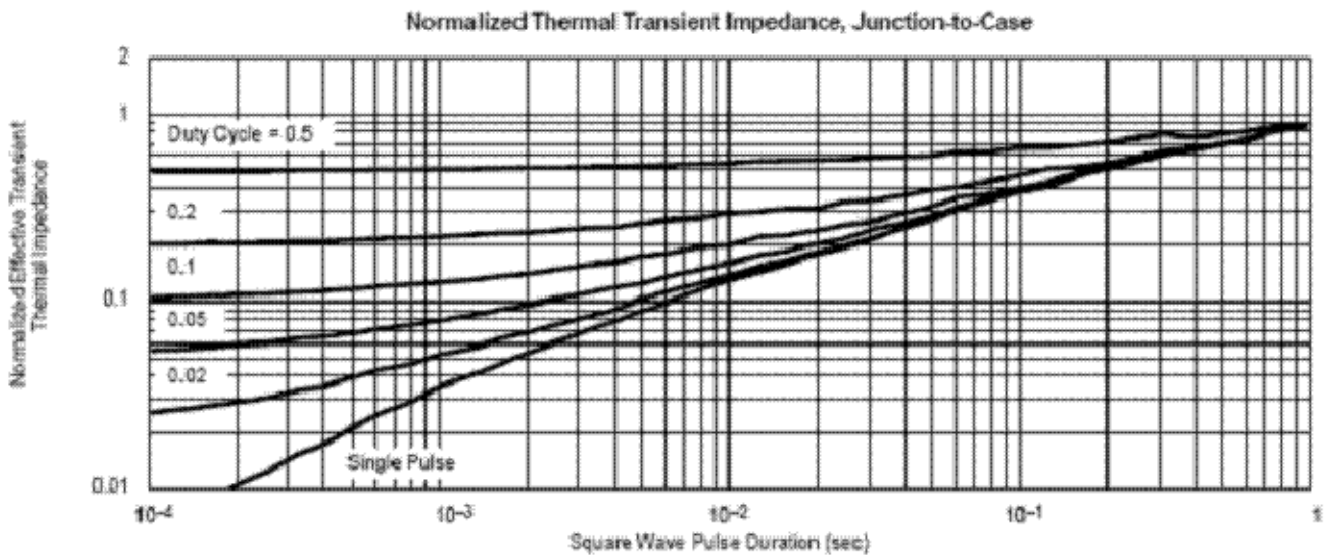
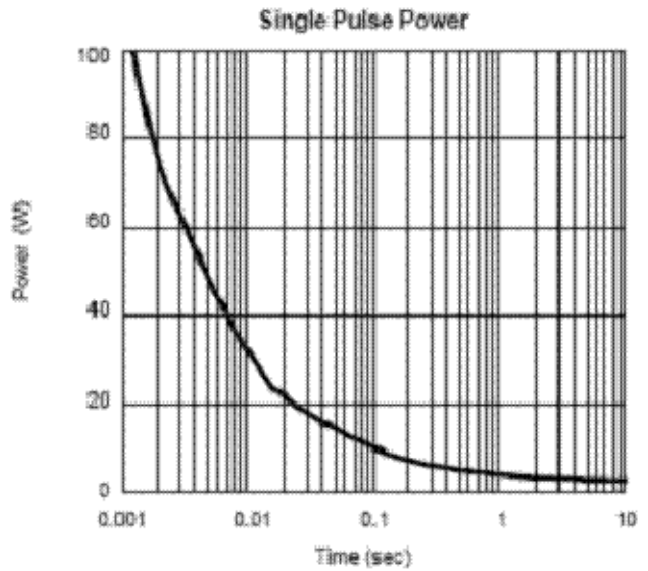
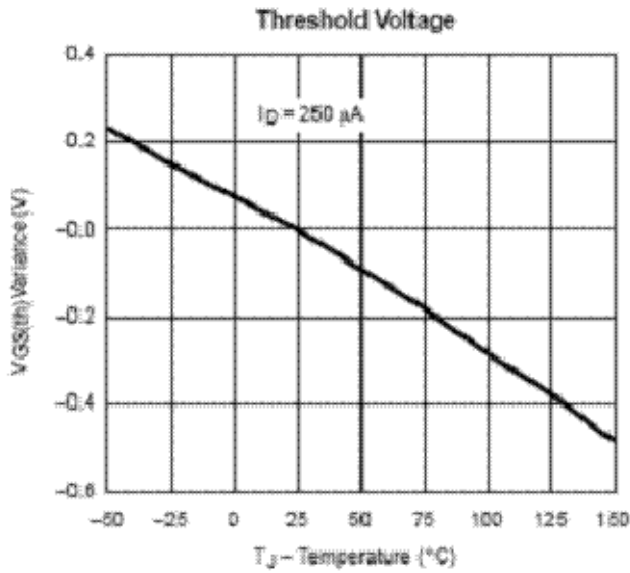
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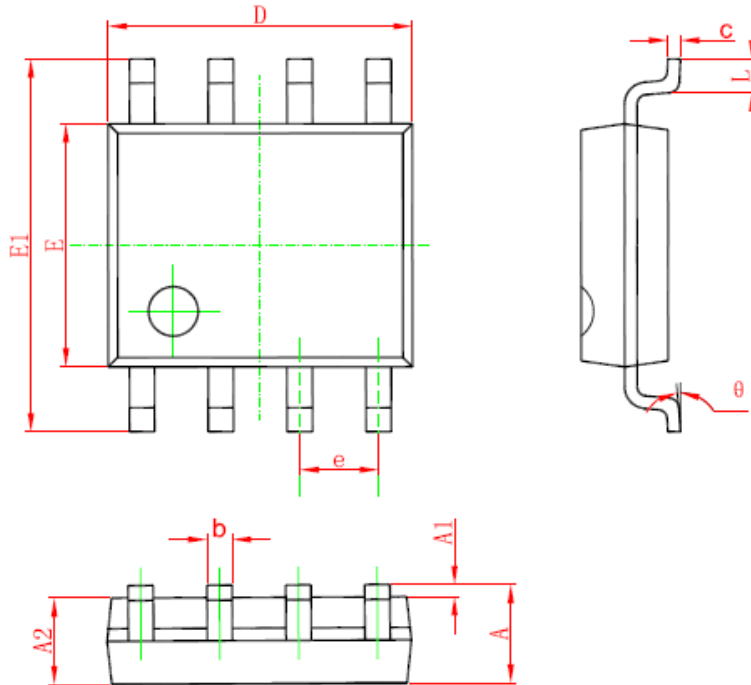
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SOP- 8 PACKAGE OUTLINE



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## N-Channel Enhancement Mode MOSFET



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°





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