



SPP2321

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP2321 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

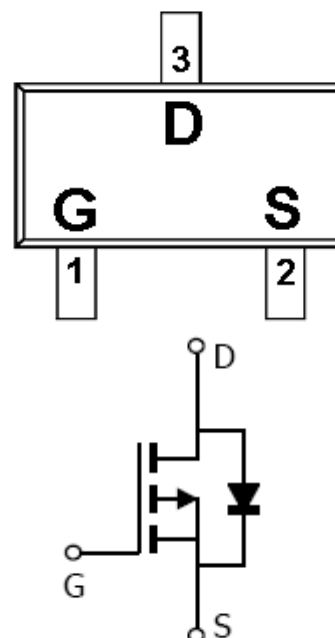
FEATURES

- ◆ $-100\text{V}/-0.6\text{A}, R_{DS(ON)}=650\text{m}\Omega @ V_{GS}=-10\text{V}$
- ◆ $-100\text{V}/-0.4\text{A}, R_{DS(ON)}=760\text{m}\Omega @ V_{GS}=-4.5\text{V}$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

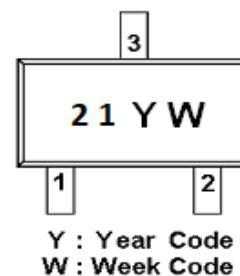
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-23)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2321S23RGB	SOT-23	21

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPP2321S23RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	-100	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	T _A =25°C	I _D	-840	mA
	T _A =70°C		-670	
Pulsed Drain Current		I _{DM}	-3.36	A
Continuous Source Current(Diode Conduction)		I _S	-1.0	A
Power Dissipation	T _A =25°C	P _D	1.25	W
	T _A =70°C		0.8	
Operating Junction Temperature		T _J	150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	120	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1.2	-1.8	-2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-80V, V _{GS} =0V			-1	uA
		V _{DS} =-80V, V _{GS} =0V T _J =125°C			-10	
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-600mA		540	650	mΩ
		V _{GS} =-4.5V, I _D =-400mA		590	760	
Gate resistance	R _g	V _{DS} =-0V, V _{GS} =0V f=1MHz		31		Ω
Forward Transconductance	g _{fs}	V _{DS} =-10V, I _D =-0.5A		2		S
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V			-1.0	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-50V, V _{GS} =-10V I _D =-500mA		4.4	8.8	nC
Gate-Source Charge	Q _{gs}			0.5	1	
Gate-Drain Charge	Q _{gd}			1.8	3.6	
Input Capacitance	C _{iss}	V _{DS} =-50V, V _{GS} =0V f=1MHz		382	760	pF
Output Capacitance	C _{oss}			29	60	
Reverse Transfer Capacitance	C _{rss}			18	36	
Turn-On Time	t _{d(on)}	V _{DD} =-50V, I _D =-0.5A, V _{GS} =-10V, R _G =3.3Ω		5	10	nS
	t _r			14.5	29	
Turn-Off Time	t _{d(off)}			20	40	
	t _f			8	16	



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TYPICAL CHARACTERISTICS

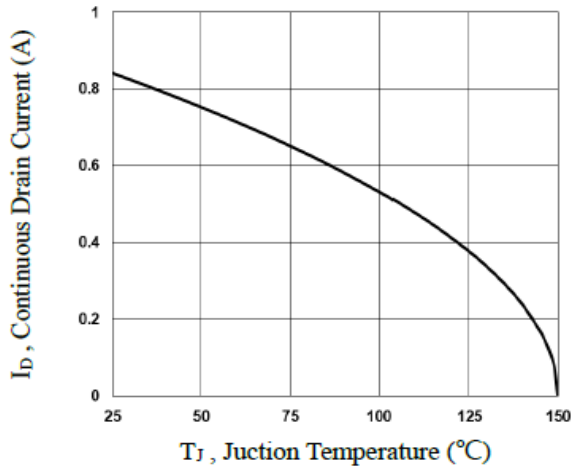


Fig.1 Continuous Drain Current vs. T_J

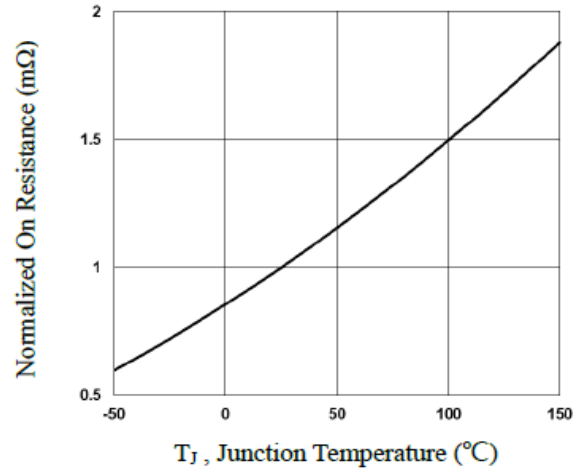


Fig.2 Normalized $R_{DS(on)}$ vs. T_J

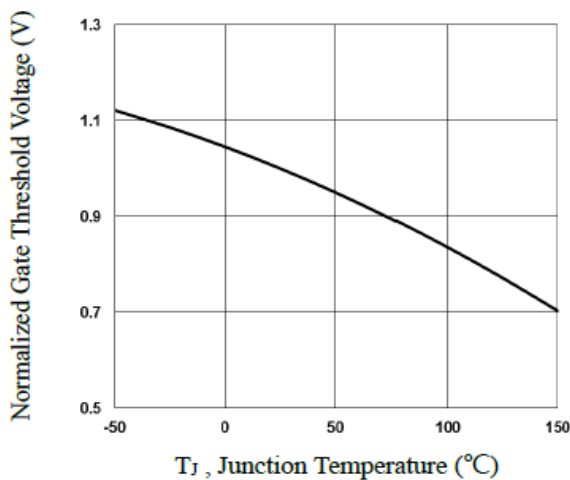


Fig.3 Normalized V_{th} vs. T_J

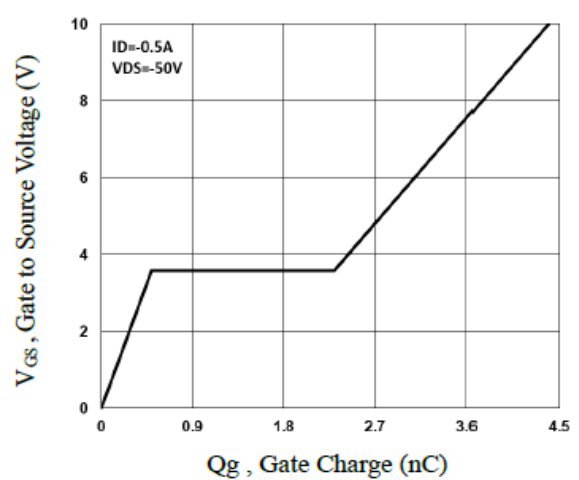


Fig.4 Gate Charge Waveform

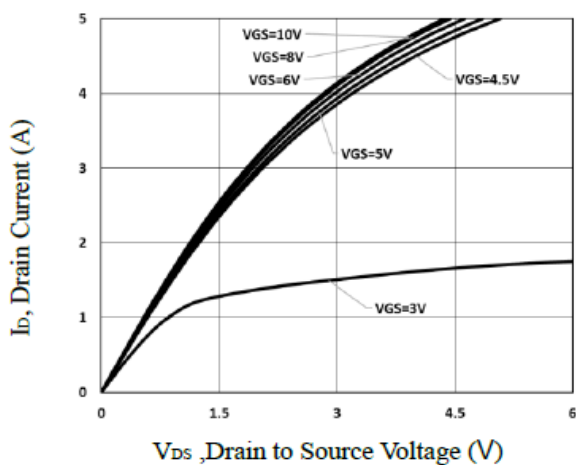


Fig.5 Typical Output Characteristics

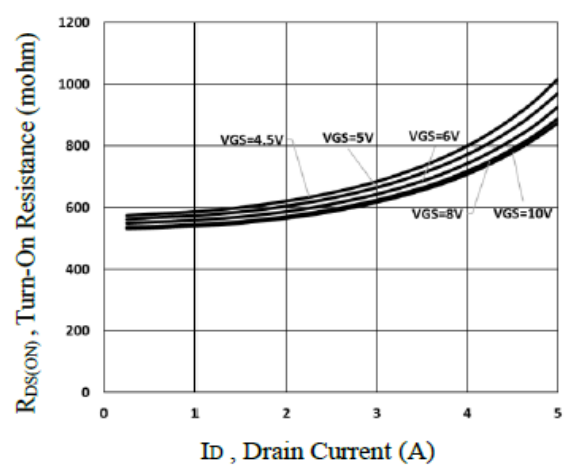


Fig.6 Turn-On Resistance vs. I_D



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TYPICAL CHARACTERISTICS

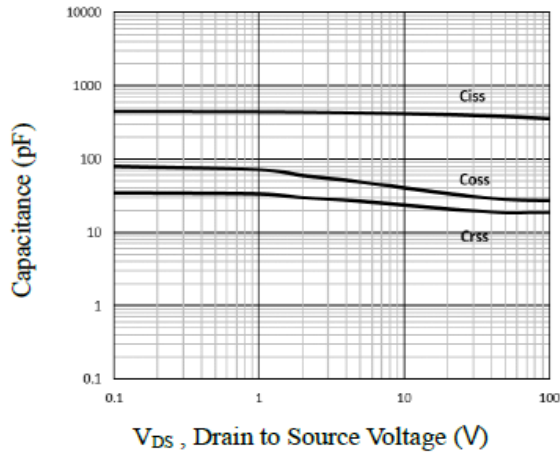


Fig.7 Capacitance Characteristics

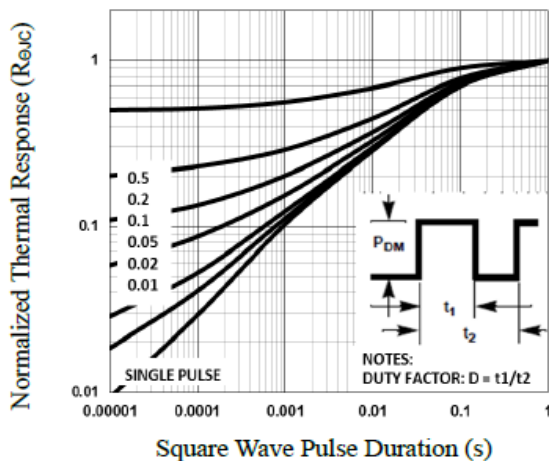


Fig.8 Normalized Transient Response

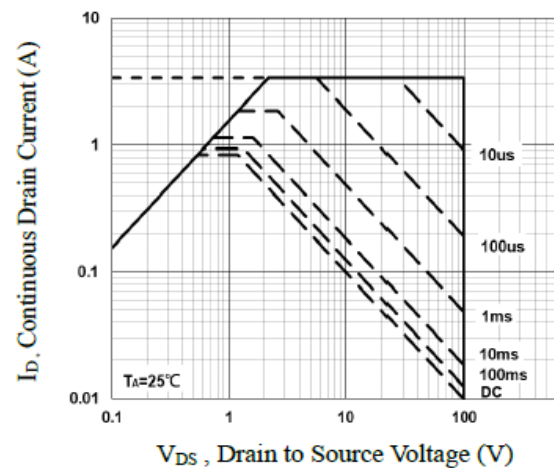


Fig.9 Maximum Safe Operation Area

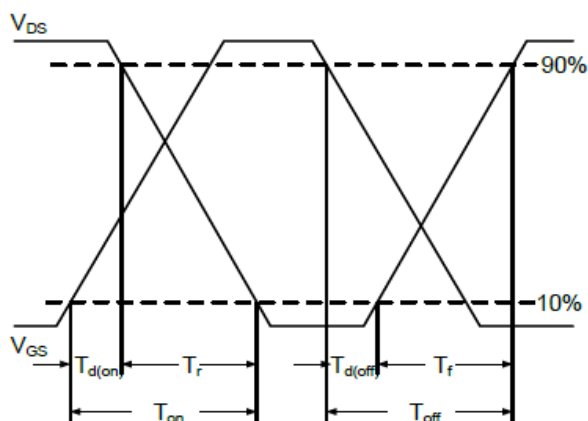


Fig.10 Switching Time Waveform

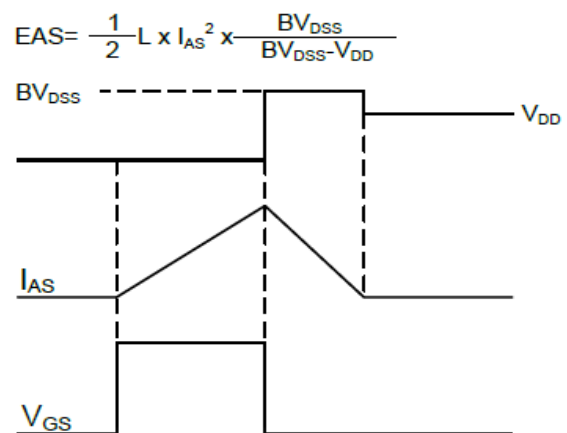


Fig.11 EAS Waveform

$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



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