SPP2325
P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP2325 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

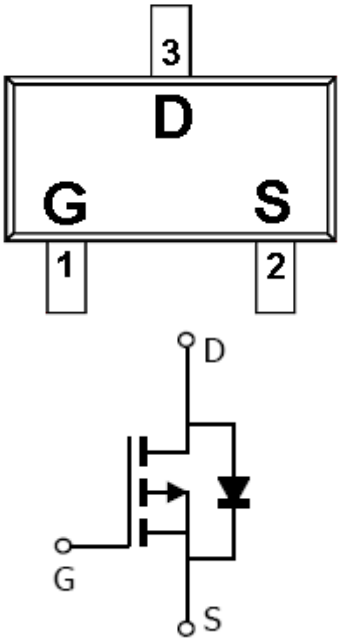
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

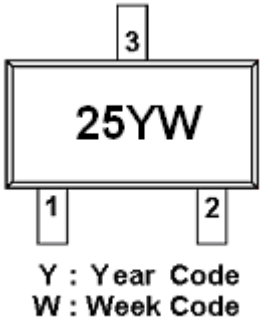
FEATURES

- -100V/-3A,$R_{DS(ON)}$=270mΩ@V_{GS}=-10V
- -100V/-1.5A,$R_{DS(ON)}$=330mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

PIN CONFIGURATION(SOT-23-3L)



PART MARKING



Y : Year Code
W : Week Code

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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2325S23RGB	SOT-23-3L	25

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPP2325S23RGB : Tape Reel ; Pb – Free; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	-3.0	A
	T_A=70℃		-2.0	
Pulsed Drain Current		I_{DM}	-4.5	A
Power Dissipation	T_A=25℃	P_D	1.15	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	100	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-1	-1.5	-2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-80V,V_{GS}=0V T_J=25℃			-10	uA
		V_{DS}=-80V,V_{GS}=0V T_J=55℃			-100	
On-State Drain Current	$I_{D(on)}$	V_{DS}=V_{GS}=0V			-3.0	A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-3A		225	270	mΩ
		V_{GS}=-4.5V,I_D=-1.5A		255	330	
Forward Transconductance	gfs	V_{DS}=-10V,I_D=-1A		2.9		S
Diode Forward Voltage	V_{SD}	I_S=-1A,V_{GS}=0V			-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-50V,V_{GS}=-10V I_D≡-1A		9.3		nC
Gate-Source Charge	Q_{gs}			1.75		
Gate-Drain Charge	Q_{gd}			1.25		
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V f=1MHz		553		pF
Output Capacitance	C_{oss}			29		
Reverse Transfer Capacitance	C_{rss}			20		
Turn-On Time	$t_{d(on)}$	V_{DD}=-50V,I_D≡-0.5A, V_{GEN}=-10V,R_G=3.3Ω		2		nS
	t_r			18.4		
Turn-Off Time	$t_{d(off)}$			19.6		
	t_f			19.5		

TYPICAL CHARACTERISTICS

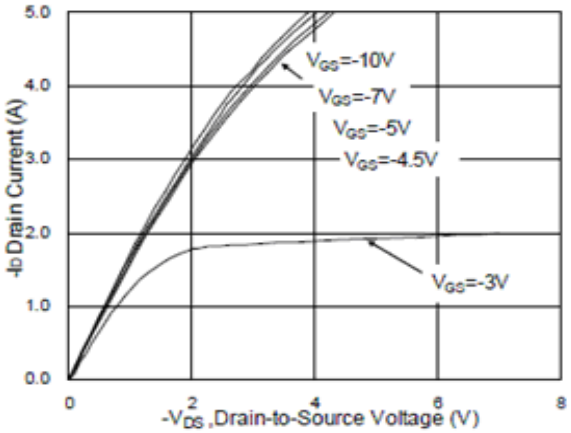

Fig 1 Output Characteristics

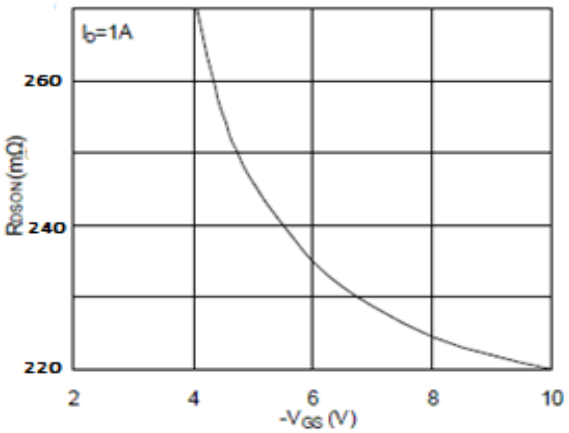

Fig. 2 On-Resistance vs Gate Source Voltage

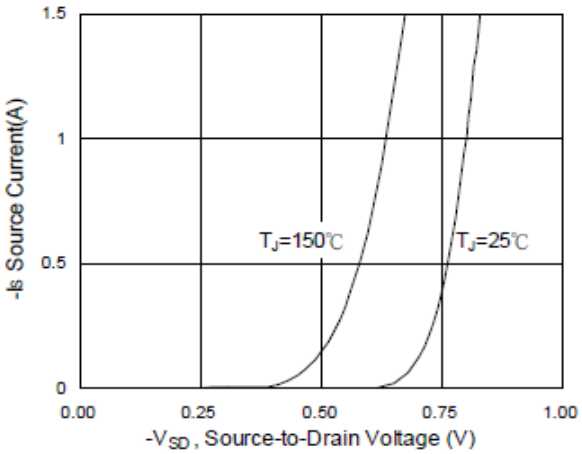

Fig 3 Source-Drain Forward Voltage

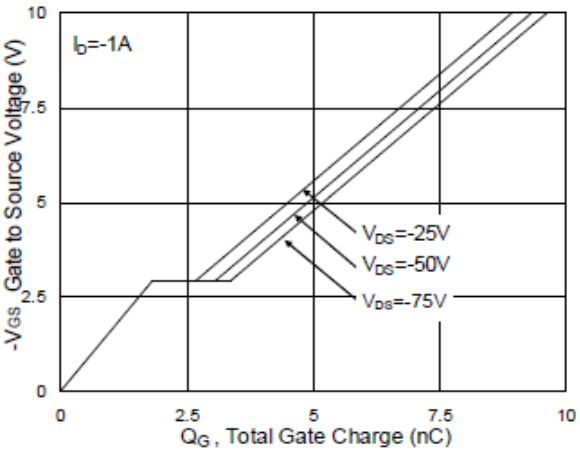

Fig. 4 Gate Charge

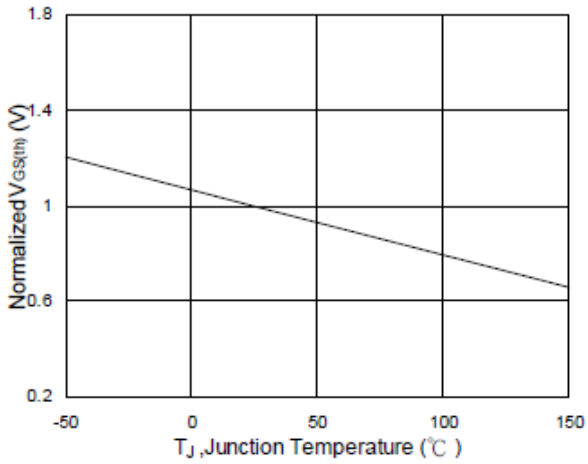

Fig. 5 Gate Voltage vs Junction temperature

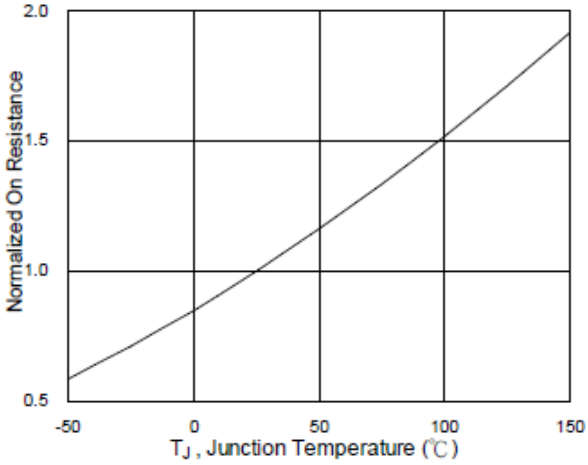

Fig. 6 On-Resistance vs Junction Temperature

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