SPP2327
P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP2327 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

APPLICATIONS

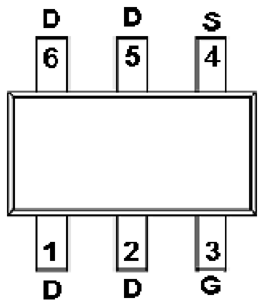
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- Networking
- LED applications

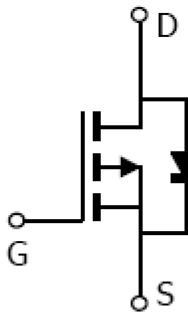
FEATURES

- -100V/-0.6A,$R_{DS(ON)}$=650mΩ@V_{GS}=-10V
- -100V/-0.4A,$R_{DS(ON)}$=760mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-6L package design

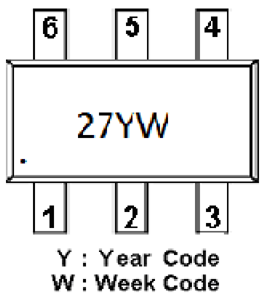
PIN CONFIGURATION

SOT-23-6L





PART MARKING



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PIN DESCRIPTION (SOT-23-6L)

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2327S26RGB	SOT-23-6L	27

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPP2327S26RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	-840	mA
	T_A=70℃		-670	
Pulsed Drain Current		I_{DM}	-3.36	A
Continuous Source Current(Diode Conduction)		I_S	-1.0	A
Power Dissipation	T_A=25℃	P_D	1.25	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	120	℃/W

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-1.2	-1.8	-2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-80V,V_{GS}=0V			-1	uA
		V_{DS}=-80V,V_{GS}=0V T_J=125℃			-10	uA
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-600mA		540	650	mΩ
		V_{GS}=-4.5V,I_D=-400mA		590	760	mΩ
Gate resistance	Rg	V_{DS}=-0V,V_{GS}=0V f=1MHz		31		Ω
Forward Transconductance	gfs	V_{DS}=-10V,I_D=-0.5A		2		S
Diode Forward Voltage	V_{SD}	I_S=-1A,V_{GS}=0V			-1.0	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-50V,V_{GS}=-10V I_D=-500mA		4.4	8.8	nC
Gate-Source Charge	Q_{gs}			0.5	1	nC
Gate-Drain Charge	Q_{gd}			1.8	3.6	nC
Input Capacitance	C_{iss}	V_{DS}=-50V,V_{GS}=0V f=1MHz		382	760	pF
Output Capacitance	C_{oss}			29	60	pF
Reverse Transfer Capacitance	C_{rss}			18	36	pF
Turn-On Time	$t_{d(on)}$	V_{DD}=-50V,I_D=-0.5A, V_{GS}=-10V,R_G=3.3Ω		5	10	nS
	t_r			14.5	29	nS
Turn-Off Time	$t_{d(off)}$			20	40	nS
	t_f			8	16	nS

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TYPICAL CHARACTERISTICS

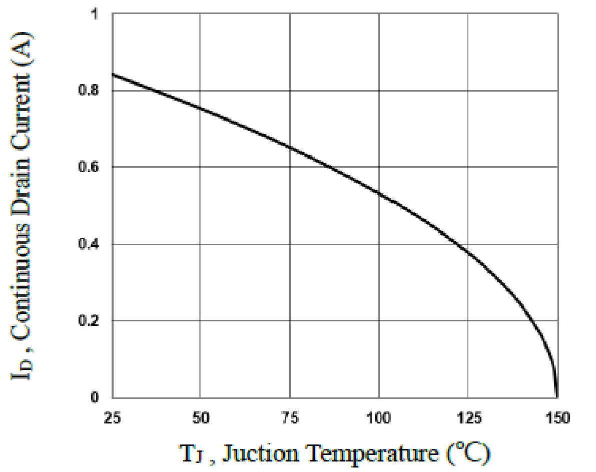

Fig.1 Continuous Drain Current vs. T_J

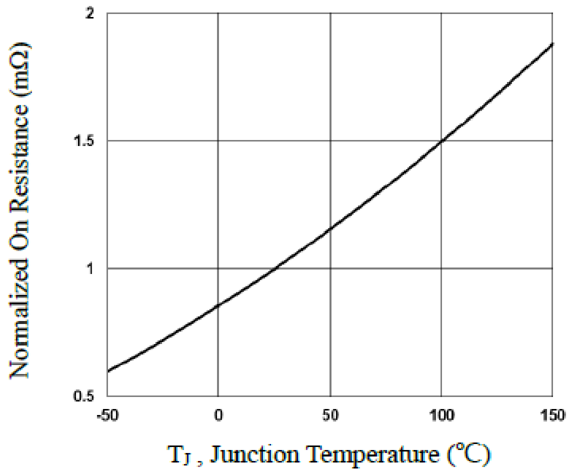

Fig.2 Normalized RDSON vs. T_J

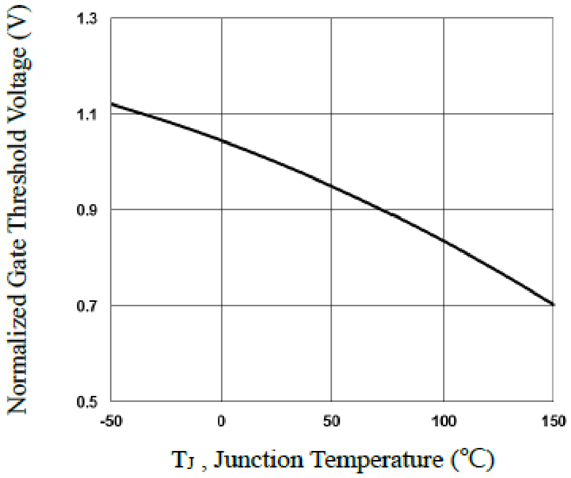

Fig.3 Normalized V_{th} vs. T_J

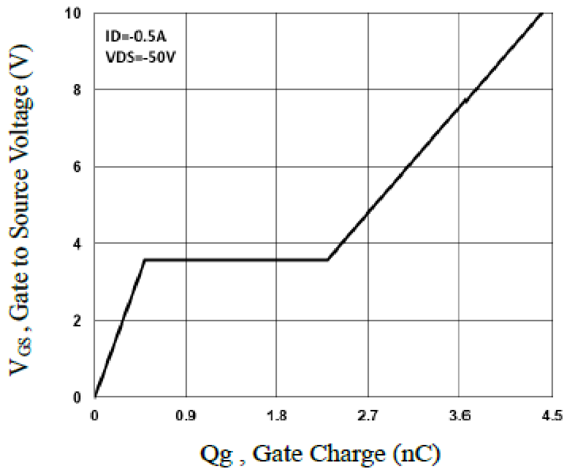

Fig.4 Gate Charge Waveform

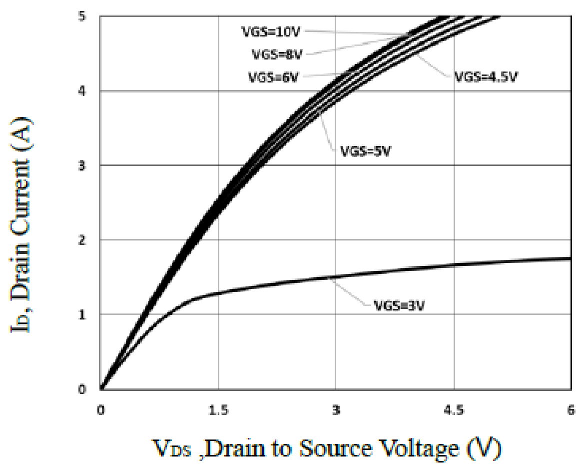

Fig.5 Typical Output Characteristics

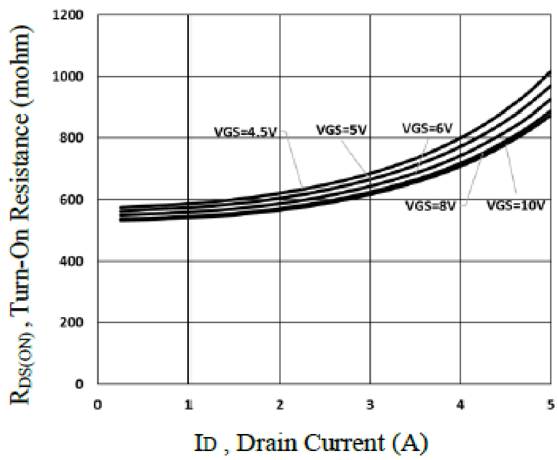

Fig.6 Turn-On Resistance vs. I_D

TYPICAL CHARACTERISTICS

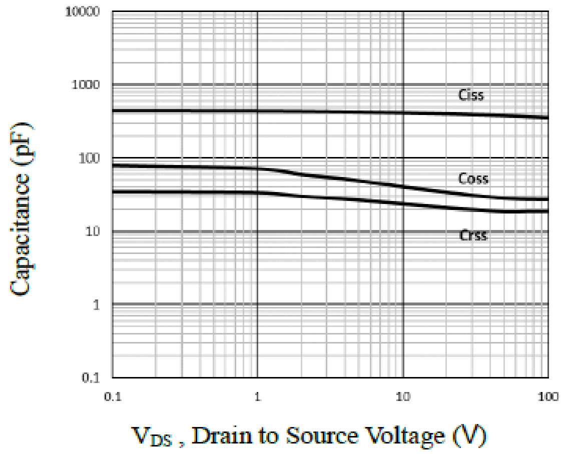

Fig.7 Capacitance Characteristics

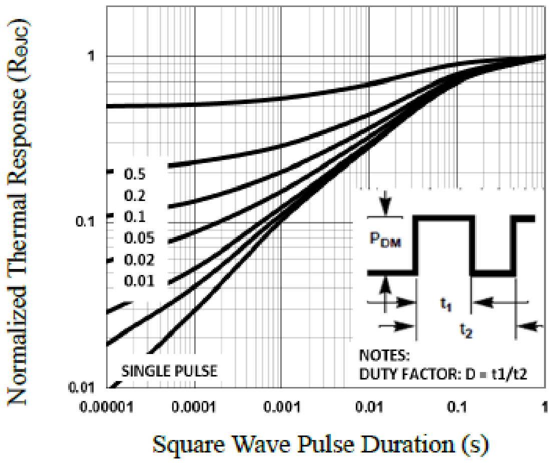

Fig.8 Normalized Transient Response

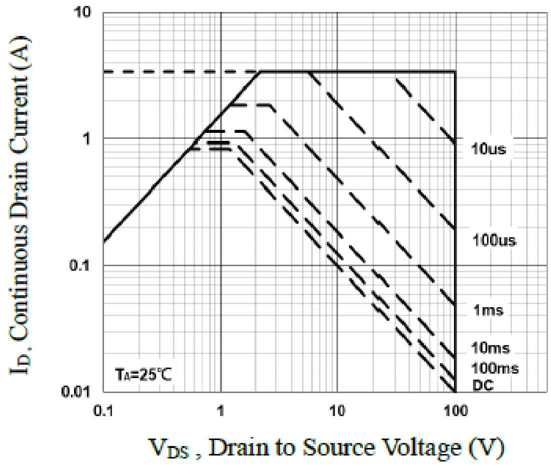

Fig.9 Maximum Safe Operation Area

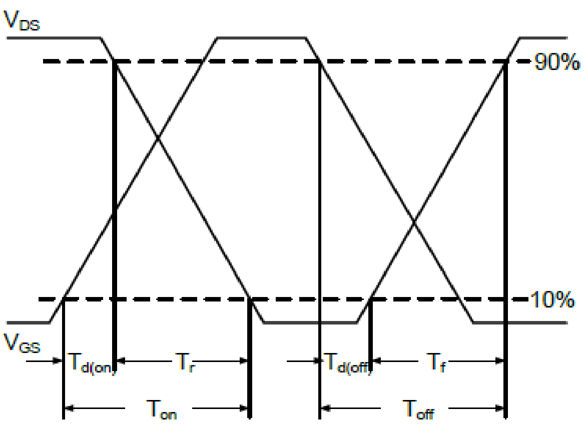

Fig.10 Switching Time Waveform

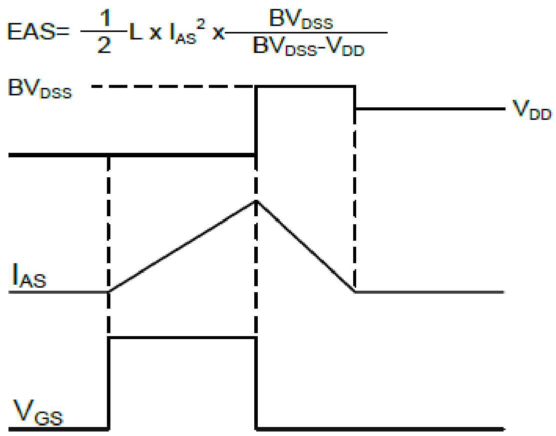

Fig.11 EAS Waveform

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