



SPP2341

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP2341 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

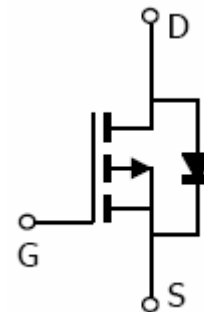
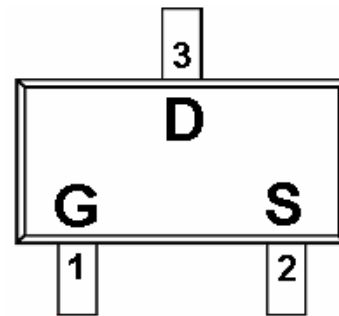
FEATURES

- ◆ -20V/-3.3 A, $R_{DS(ON)} = 45m\Omega @ V_{GS} = -4.5V$
- ◆ -20V/-2.8 A, $R_{DS(ON)} = 55m\Omega @ V_{GS} = -2.5V$
- ◆ -20V/-2.3 A, $R_{DS(ON)} = 65m\Omega @ V_{GS} = -1.8V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23-3L package design

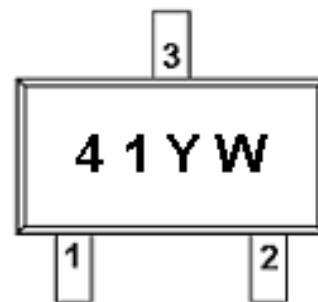
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-23-3L)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2341S23RG	SOT-23-3L	41YW
SPP2341S23RGB	SOT-23-3L	41YW

- ※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
- ※ SPP2341S23RG : Tape Reel ; Pb – Free
- ※ SPP2341S23RGB : Tape Reel ; Pb – Free ; Halogen – Free
- ※

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-20	V	
Gate –Source Voltage	V _{GSS}	±12	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-4.0	A
		TA=70°C	-2.8	
Pulsed Drain Current	I _{DM}	-12	A	
Continuous Source Current(Diode Conduction)	I _S	-1.0	A	
Power Dissipation	P _D	TA=25°C	1.25	W
		TA=70°C	0.8	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	140	°C/W	



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ELECTRICAL CHARACTERISTICS

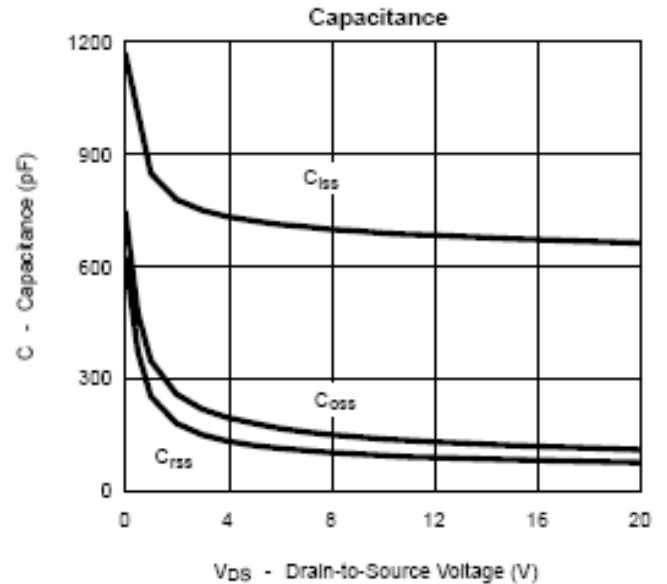
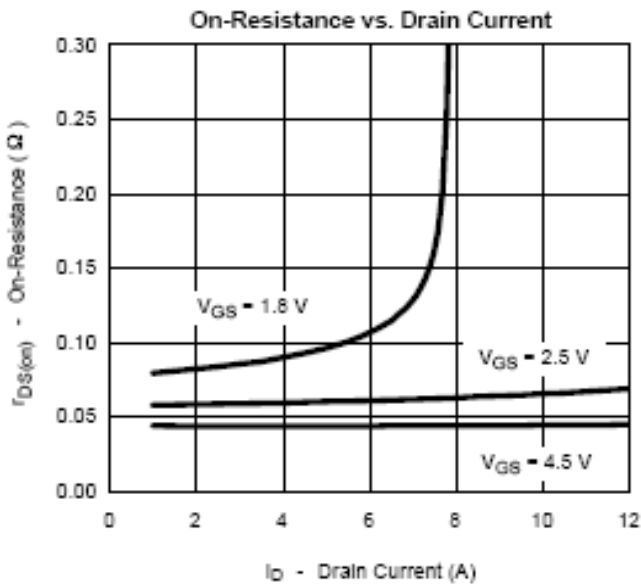
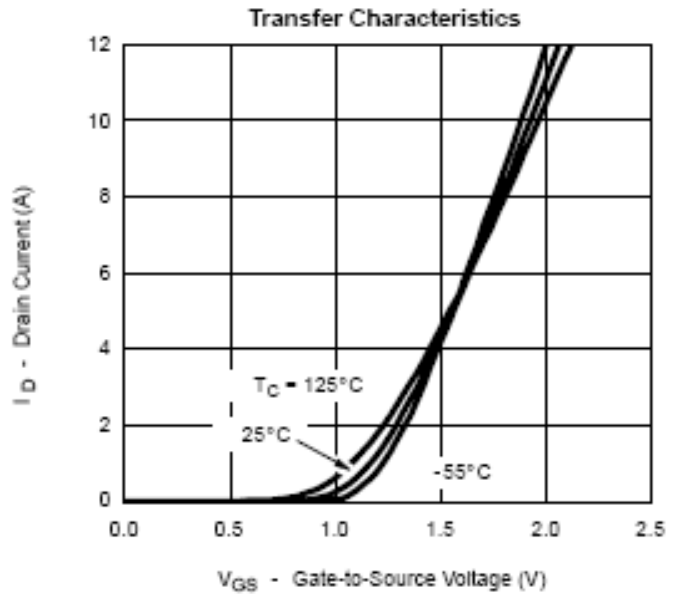
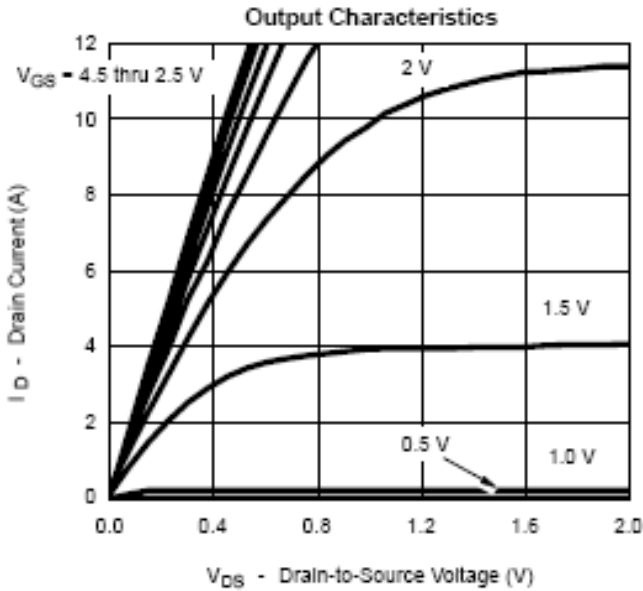
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.35		-0.9	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$			-1	uA
		$V_{DS}=-20V, V_{GS}=0V$ $T_J=55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq -5V, V_{GS}=-4.5V$	-6			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-3.3A$		0.036	0.045	Ω
		$V_{GS}=-2.5V, I_D=-2.8A$		0.045	0.055	
		$V_{GS}=-1.8V, I_D=-2.3A$		0.055	0.065	
Forward Transconductance	g_{fs}	$V_{DS}=-5.0V, I_D=-3.3A$		3		S
Diode Forward Voltage	V_{SD}	$I_S=-1.6A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-6V, V_{GS}=-4.5V$ $I_D=-3.3A$		8	13	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			2.2		
Input Capacitance	C_{iss}	$V_{DS}=-6V, V_{GS}=0V$ $f=1MHz$		700		pF
Output Capacitance	C_{oss}			160		
Reverse Transfer Capacitance	C_{rss}			120		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-6V, R_L=6\Omega$ $I_D=-1.0A, V_{GEN}=-4.5V$ $R_G=6\Omega$		15	25	ns
	t_r			35	55	
Turn-Off Time	$t_{d(off)}$			60	90	
	t_f			40	60	



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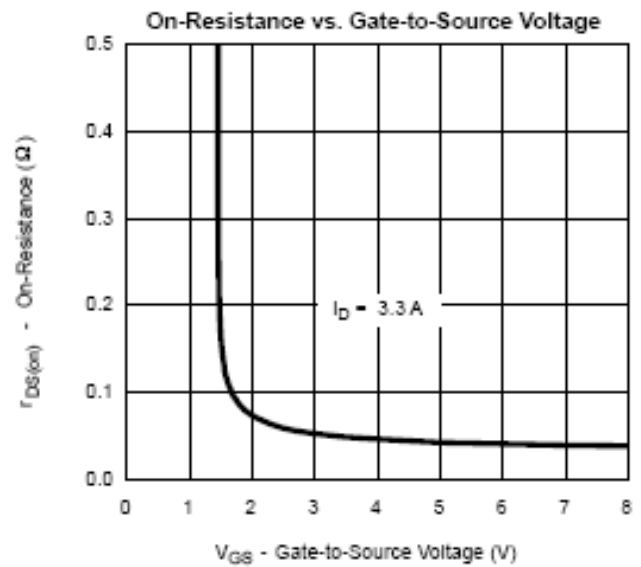
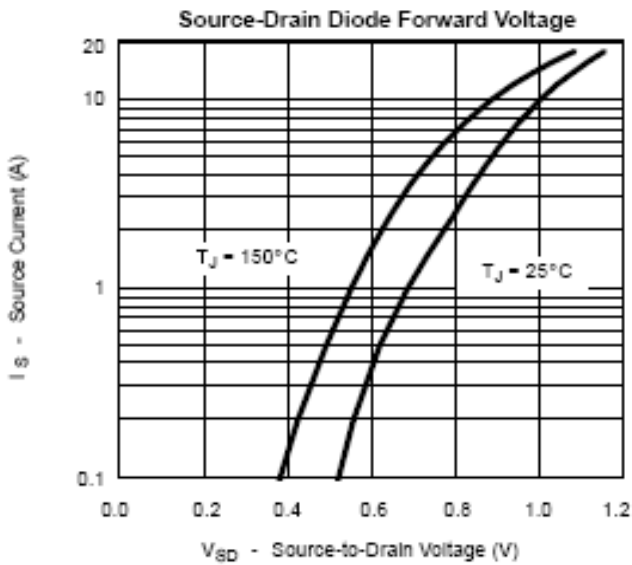
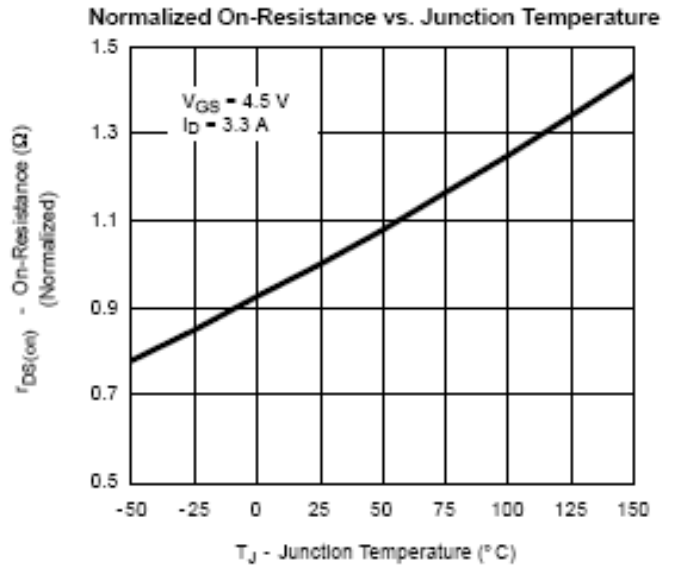
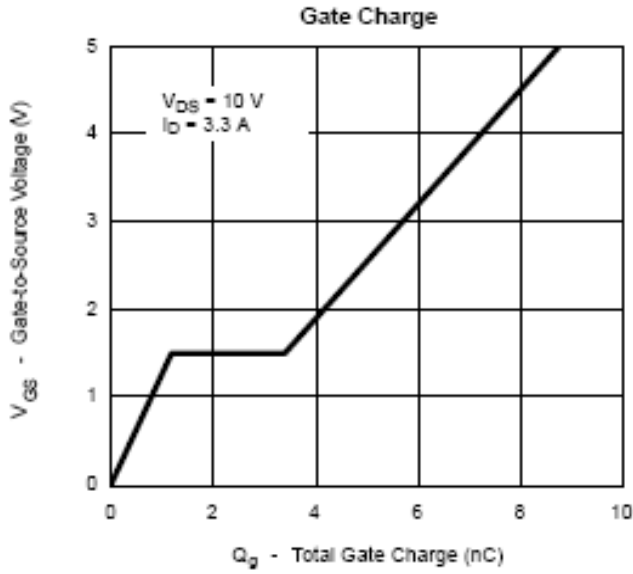
TYPICAL CHARACTERISTICS





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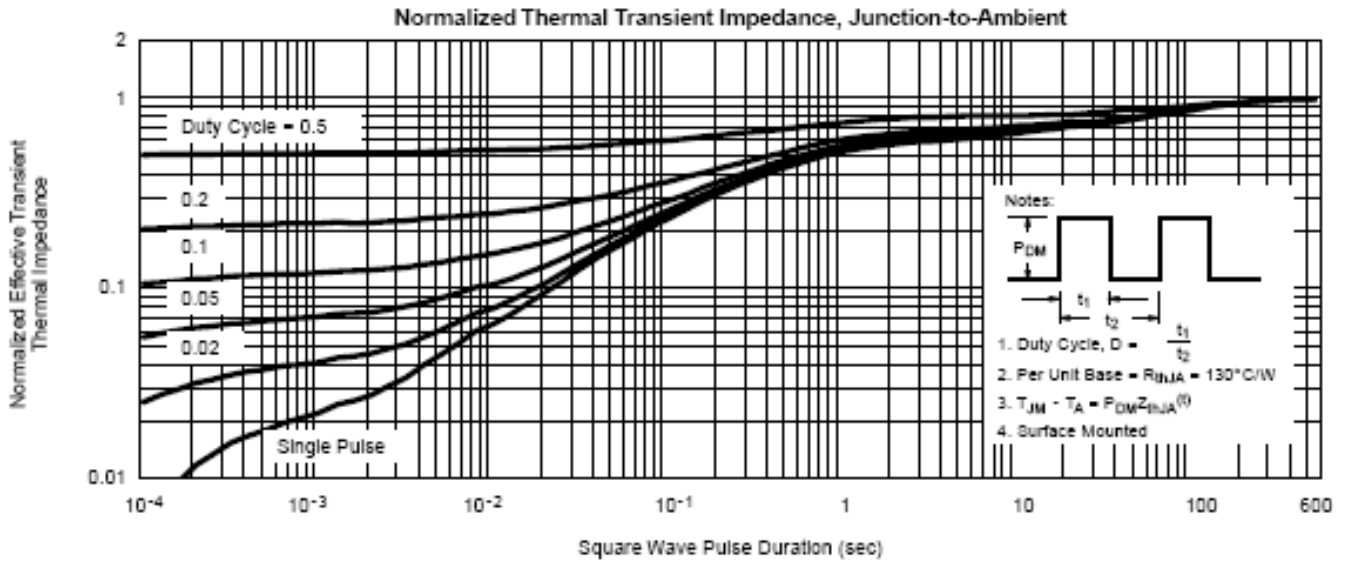
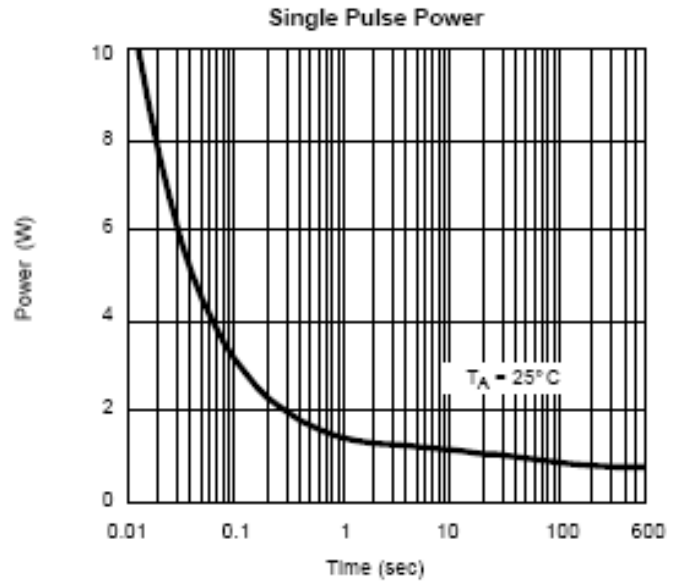
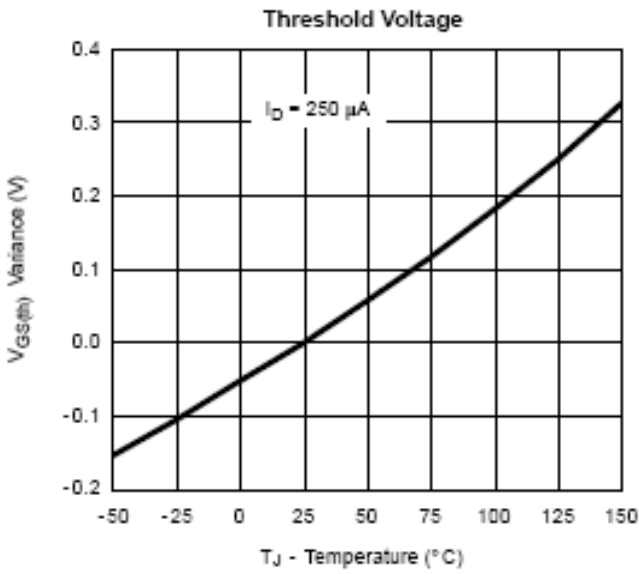




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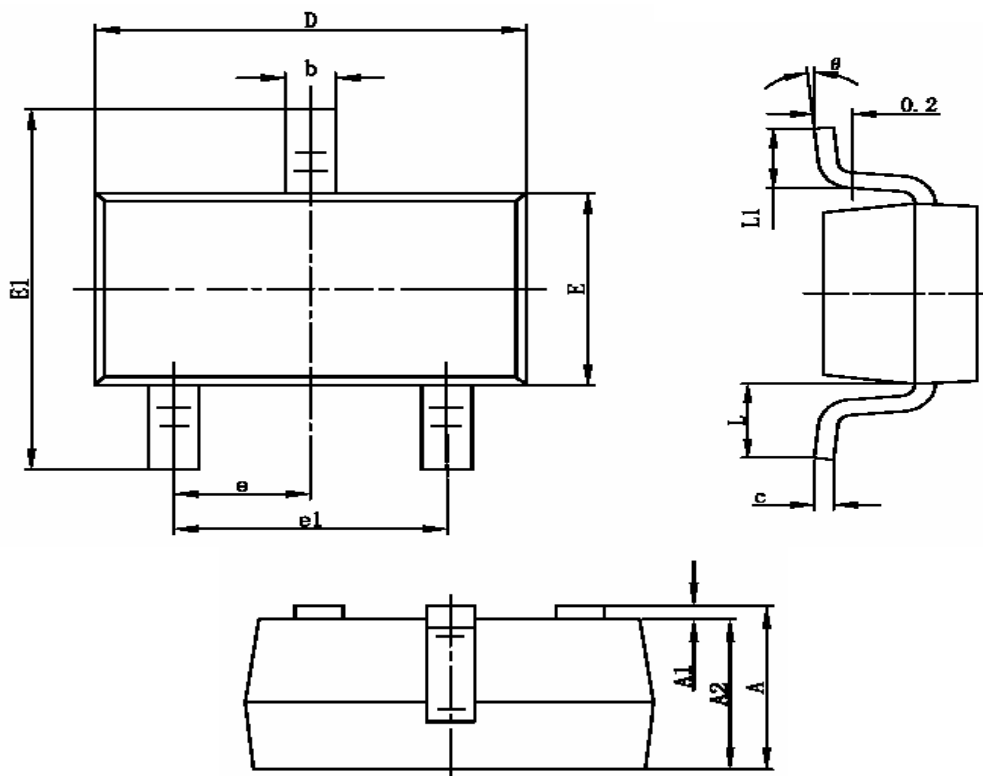




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SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
theta	0°	8°	0°	8°



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